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An Improved New Technique to Compensate Reactive and Nonlinear Loads by Hybrid DSTATCOM Topology

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Abstract

This project presents a control algorithm based on enhanced phase locked loop (EPLL) for distribution static compensator (DSTATCOM) to compensate reactive power, to provide load balancing, to eliminate harmonics, to correct power factor, and to regulate point of common coupling (PCC) voltages. Under linear and nonlinear loads An LCL filter has been used at the front end of a voltage source inverter (VSI), which provides better switching harmonics elimination while using much smaller value of an inductor as compared with the traditional L filter. A capacitor is used in series with an LCL filter to reduce the dc-link voltage of the DSTATCOM. This consequently reduces the power rating of the VSI. With reduced dc-link voltage, the voltage across the shunt capacitor of the LCL filter will be also less. It will reduce the power losses in the damping resistor as compared with the traditional LCL filter with passive damping. Therefore, the proposed DSTATCOM topology will have reduced weight, cost, rating, and size with improved efficiency and current compensation capability compared with the traditional topology. A systematic procedure to design the components of the passive filter has been presented. The effectiveness of the proposed DSTATCOM topology over traditional topologies is validated through both simulation and experimental studies.

Index Terms—*Distribution static compensator (DSTATCOM), hybrid topology, passive filter, power quality (PQ).*

I. INTRODUCTION

The quality of available supply power has a direct economic impact on industrial and domestic sectors which affects the growth of any nation [1]. This issue is more serious in electronic based systems. The level of harmonics and reactive power demand are popular parameters that specify the degree of distortion and reactive power demand at a particular bus of the utility [2]. The harmonic resonance is one of the most common problems reported in low and medium-level distribution systems. It is due to capacitors which are used for power factor correction (PFC) and source impedance [3]. Power converter-based custom power devices (CPDs) are useful for the reduction of power quality problems such as PFC, harmonic compensation, voltage sag/swell compensation, resonance due to distortion, and voltage flicker reduction within specified international standards [4]–[6]. These (CPDs) include the distribution static compensator (DSTATCOM), dynamic voltage restorer, and unified power quality conditioner in different configurations [7]–[9]. Some of their new topologies are also reported in the literature such as the indirect matrix converter based active compensator where the dc-link capacitor can be removed [10]. Other new configurations are based on stacked multi cell converters where the main features are on the increase in the number of output voltage levels, without transformer operation and natural self-balancing of flying capacitor voltage, etc. [11]. The performance of any custom power device depends very much upon the control algorithm used for the reference current estimation and gating pulse generation scheme. However, a traditional DSTATCOM requires a high-power

rating voltage source inverter (VSI) for load compensation. The power rating of the DSTATCOM is directly proportional to the current to be compensated and the dc-link voltage [9]. Generally, the dc-link voltage is maintained at much higher value than the maximum value of the phase-to-neutral voltage in a three-phase four-wire system for satisfactory compensation (in a three-phase three-wire system, it is higher than the phase-to-phase voltage) [2],[10]–[12]. However, a higher dc-link voltage increases the rating of the VSI, makes the VSI heavy, and results in higher voltage rating of insulated gate bipolar transistor (IGBT) switches. It leads to the increase in the cost, size, weight, and power rating of the VSI. In addition, traditional DSTATCOM topologies use an L-type interfacing filter for shaping of the VSI injected currents [13], [14]. The L filter uses a large inductor, has a low slew rate for tracking the reference currents, and produces a large voltage drop across it, which, in turn, requires a higher value of the dc-link voltage for proper compensation. Therefore, the L filter adds in cost, size, and power rating. Some hybrid topologies have been proposed to consider the aforementioned limitations of the traditional DSTATCOM, where a reduced rating active filter is used with the passive components [15]–[21]. In [15] and [16], hybrid filters for motor drive applications have been proposed. In [17], authors have achieved a reduction in the dc-link voltage for reactive load compensation. However, the reduction in voltage is limited due to the use of an L-type interfacing filter. This also makes the filter bigger in size and has a lower slew rate for reference tracking. An LCL filter has been proposed as the front end of the VSI in the literature to overcome the limitations of an L filter [22]–[25]. It provides better reference tracking performance while using much lower value of passive components. This also reduces the cost, weight, and size of the passive component. However, the LCL filter uses a similar dc-link voltage as that of DSTATCOM employing an L filter. Hence, disadvantages due to high dc-link voltage are still present when the LCL filter is used. Another serious issue is resonance damping of the LCL filter, which may push the system toward instability. One solution is to use active damping. This can be achieved using either additional sensors or sensorless schemes. The sensorless active damping scheme is easy to implement by modifying the inverter control structure. It eliminates the need for additional sensors. However, higher order digital filters used in these schemes may require to be tuned for satisfactory performance [26]. Another approach is to go for passive damping. This does not require extra sensor circuitry. However, insertion of a damping resistor in the shunt part of an LCL filter results in extra power loss and reduces the efficiency of the system [26]. This paper proposes an improved hybrid DSTATCOM topology where the LCL filter followed by the series capacitor is used at the front end of the VSI to address the aforementioned issues. This topology reduces the size of the passive components and the rating of the dc-link voltage and provides good reference tracking performance simultaneously. Along with this, a significant reduction in the damping power loss is achieved, which makes this scheme suitable for industrial applications. The performance of the proposed topology is validated through the extensive simulation and experimental results.

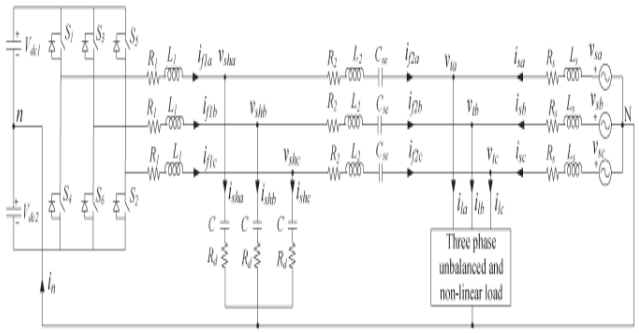

Fig 1. Proposed DSTATCOM topology in the distribution system to compensate unbalanced and nonlinear loads

II. PROPOSED DSTATCOM TOPOLOGY

The proposed topology enables DSTATCOM to have a reduced dc-link voltage without compromising the compensation capability. It uses a series capacitor along with the interfacing inductor and a shunt filter capacitor. With the reduction in dc-link voltage, the average switching frequency of the

insulated gate bipolar transistor switches of the DSTATCOM is also reduced. Consequently, the switching losses in the inverter are reduced. Detailed design aspects of the series and shunt capacitors are discussed in this paper. A simulation study of the proposed topology has been carried out using power systems computer-aided design simulator and the results are presented. Experimental studies are carried out to verify the proposed topology A three-phase equivalent circuit diagram of the proposed DSTATCOM topology is shown in Fig. 1. It is realized using a three-phase four-wire two-level neutral-point-clamped VSI. The proposed scheme connects an LCL filter at the front end of the VSI, which is followed by a series capacitor Cse. Introduction of the LCL filter significantly reduces the size of the passive component and improves the reference tracking performance. Addition of the series capacitor reduces the dc-link voltage and, therefore, the power rating of the VSI. Here, R1 and L1 represent the resistance and inductance, respectively, at the VSI side; R2 and L2 represent the resistance and inductance, respectively, at the load side; and C is the filter capacitance forming the LCL filter part in all three phases. A damping resistance Rd is used in series with C to damp out resonance and to provide passive damping to the overall system. VSI and filter currents are if1a and if2a, respectively, in phase-a and similar for other phases. In addition, voltages across and currents through the shunt branch of the LCL filter in phase-a are given by vsha and isha, respectively, and similarly for the other two phases. The voltages maintained across the dc-link capacitors are Vdc1 = Vdc2 = Vdcref . The DSTATCOM, source, and loads are connected to a common point called the point of common coupling (PCC). Loads used here have both linear and nonlinear elements, which may be balanced or unbalanced. In the traditional DSTATCOM topology considered in this paper, the same VSI is connected to the PCC through an inductor Lf [27]. In the LCL filter-based DSTATCOM topology, an LCL filter is connected between the VSI and the PCC [22].

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III. DSTATCOM CONTROL

The overall control block diagram is shown in Fig. 2. The DSTATCOM is controlled in such a way that the source currents are balanced, sinusoidal, and in phase with the respective terminal voltages. In addition, average load power and losses in the VSI are supplied by the source. Since the source considered

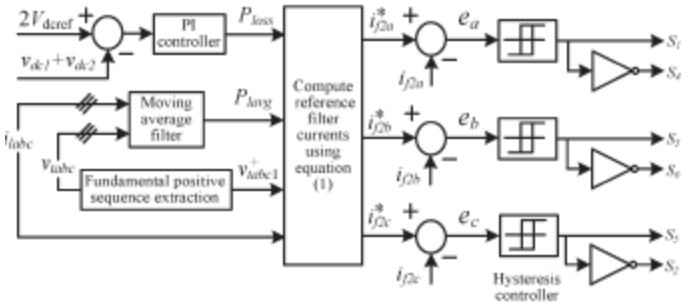


Fig. 2. Controller block diagram

Here is non stiff, the direct use of terminal voltages to calculate reference filter currents will not provide satisfactory compensation. Therefore, the fundamental positive sequence components of three-phase voltages are extracted to generate reference filter currents (i∗ f2a, i∗ f2b, and i∗ f2c) based on the instantaneous symmetrical component theory [27]. These currents are given as follows:

$$\mathbf{i^*_{f2a} = i_{la} - i^*_{sa} = i_{la} - \frac{v^+_{ta1}}{\Delta^+_1}\left(P_{lavg} + P_{loss}\right)}$$

$$\mathbf{i^*_{f2b} = i_{lb} - i_{sb} = i_{lb} - \frac{v^+_{tb1}}{\Delta^+_1}\left(P_{lavg} + P_{loss}\right)}$$

$$\mathbf{i^*_{f2c} = i_{lc} - i_{sc} = i_{lc} - \frac{v^+_{tc1}}{\Delta^+_1}\left(P_{lavg} + P_{loss}\right)} \quad (1)$$

where v+ta1, v+tb1, and v+tc1 are fundamental positive sequence voltages at the respective phase load terminal, and Δ+1 = (v+ta1)2 + (v+tb1)2 + (v+tc1)2. The terms Plavg and Ploss represent the average load power and the total losses in the VSI, respectively. The average load power is calculated using a moving average filter for better performance during transients and can have a window width of half-cycle or full cycle depending upon the odd or odd and even harmonics, respectively, present in the load currents. At any arbitrary time t1, it is computed as follows:

$$P_{lavg} = \frac{1}{T}\int_{t1-T}^{t1} (v_{ta}i_{la} + v_{tb}i_{lb} + v_{tc}i_{lc})dt \quad (2)$$

The total losses in the VSI are computed using a proportional–integral (PI) controller at the positive zero crossing of phase-a voltage. It helps in maintaining the dc-link voltage vdc1 + vdc2 at a reference value 2Vdcref by drawing a set of balanced currents from the source and is given as

$$P_{loss} = K_p e_{vdc} + K_i \int e_{vdc}\, dt \quad (3)$$

where Kp, Ki, and evdc = 2Vdcref − (vdc1 + vdc2) are the proportional gain, integral gain, and voltage error of the PI controller, respectively. The current error eabc is obtained by subtracting the actual filter currents from the reference filter currents. The error is regulated around a predefined hysteresis band h using the hysteresis current controller (HCC), and IGBT switching pulses are generated.

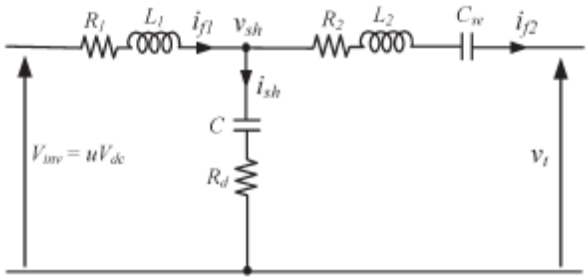


Fig. 3. Single-phase circuit diagram of the passive filter

IV. DSTATCOM PARAMETER DESIGN

The dc bus voltage and interfacing filter values of the traditional DSTATCOM are calculated based on the procedure outlined in [28]. For a supply voltage of 230 V, a load rating of 10 kVA, a maximum switching frequency of 10 kHz, and a ripple current of 1 A (5% of the rated current), the dc-link voltage and interfacing inductor values are found to be 520 V and 26 mH, respectively. For the LCL filter based DSTATCOM topology, the dc bus voltage and filter parameters are chosen for the same set of design requirements [22], [23], [28]. The single-phase equivalent circuit diagram of the passive filter of the proposed scheme connected to the PCC is shown in Fig. 3. The term uVdc represents the inverter pole voltage with u as a switching variable having a value of +1 or −1 depending upon the switching states. The procedure to design the filter parameters is given here in detail. 1) Reference DC-Link Voltage Vdcref : The voltage across the dc capacitor is a source of energy and is selected to achieve good tracking performance. Here, the use of a series capacitor and a small filter inductor has enabled a significant reduction in the dc-link voltage. In present case, a dc-link voltage of 110 V is chosen, which is found to provide satisfactory compensation. 2) Design of LCL Filter Parameters: While designing suitable values of LCL filter components, constraints such as cost of inductor, resonance frequency fres, choice of damping resistor Rd, and attenuation at switching frequency fsw should be considered [22], [23]. Consider only L1 of the passive filter, as shown in Fig. 3, is used. The value of inductance L1 is chosen from a tradeoff, which provides a reasonably high switching frequency and a sufficient rate of change of the filter current, such that the VSI currents follow the reference currents. At any point of time, the following equation represents the inductor dynamics:

$$L_1 \frac{di_{f1}}{dt} = -v_t - R_1 i_{f1} + V_{dcref} \quad (4)$$

For further analysis, R1 can be neglected. The inductor is designed to provide good tracking performance at maximum switching frequency, which is achieved at zero supply voltage in the HCC [28]. Taking these into consideration, inductance L1 is given by

$$L_1 = \frac{V_{dcref}}{(2h_o)(2f_{max})} = \frac{V_{dcref}}{4h_0} \quad (5)$$

where 2ha is allowable ripple in the current, and fmax is the maximum switching frequency achieved by the HCC. The large ripple current will lower the IGBT switching frequency and lowers the losses. However, it can be seen from (5) that the smaller ripple current results in higher inductance and, thus, more core losses. Therefore, a ripple current of 20% is taken while compromising the ripple and inductor size. The use of a series capacitor has reduced the dc-link voltage to 110 V. Therefore, substituting the values of the ripple current and reference dc-link voltage Vdcref in (5) while keeping fmax constant at

10 kHz, the value of L1 comes out to be 1.375 mH. To restrict the switching frequency below 10 kHz, L1 is taken more than the calculated value, therefore, 1.5 mH is chosen. Once L1 is chosen to attenuate lower order harmonics, L2 and C need to be designed for elimination of higher order harmonics. At higher frequencies, the impedance offered by Cse will be much lower than that of L2 and can be neglected while designing LCL filter parameters. Neglecting R1, R2, and Cse at higher frequencies, the following transfer functions are obtained:

$$\frac{\mathbf{I_{f1}(s)}}{\mathbf{V_{inv}(s)}} = \frac{\mathbf{s^2 + \frac{1}{L_2C}}}{\mathbf{sL_1\left(s^2 + \left(\frac{L_1 + L_2}{L_1L_2C}\right)\right)}} \quad (6)$$

$$\frac{\mathbf{I_{f2}(s)}}{\mathbf{V_{inv}(s)}} = \frac{\mathbf{\frac{1}{L_1L_2C}}}{\mathbf{s\left(s^2 + \left(\frac{L_1 + L_2}{L_1L_2C}\right)\right)}} \quad (7)$$

From (6), the expression for resonance frequency will be

$$\mathbf{f_{res} = \frac{1}{2\pi}\sqrt{\frac{1+k}{kL_1C}}} \quad (8)$$

where k = L2/L1. The resonance frequency must be greater than the highest order harmonic of the current to be compensated. If the highest harmonics order to be compensated is 40 and taking a variation of 20%, fres turns out to be 2400 Hz for a 50-Hz system. Selection of L2 > L1 (i.e., k > 1) will reduce the capability of L1 to attenuate lower order harmonics. Therefore, lower order harmonics will be also attenuated by inductor L2 to achieve satisfactory compensation performance. Usually, the magnitude of the lower order harmonics in the LCL filter is used to be more as compared with the higher order harmonics. Hence, the current through the shunt capacitor and the inductor L1 will increase for k>1. This will increase the damping power losses, the reactive power loss in inductor L1, and the inverter current. Moreover, the source current will also increase as the damping power losses are extracted from the source. Hence, L2 > L1 will result in more losses and cost. Therefore, to ensure low loss and high efficiency, a lower value of k is selected (k < 1). A higher C will provide a low impedance path for harmonics but will draw more reactive current from the VSI, which further increases the loss in L1 and IGBT switch. However, a smaller capacitance will not provide sufficient attenuation, which, in turn, is compensated by selecting a larger inductor. As a tradeoff between these requirements, C = 10 μF is chosen. The value of k is found to be 0.42 using (8). With this value of k, L2 will be 0.6 mH. The equivalent impedance of the LCL filter approaches to zero at the resonance frequency fres, and the system may become unstable. However, the system can be made stable by inserting a resistance Rd in series with the capacitor. Usually, it is chosen in proportion to the capacitive reactance at fres, i.e., Xcres, such that the damping losses are minimum while assuring system stability. The capacitive reactance at resonance will be

$$\mathbf{X_{cres} = \frac{1}{2\pi f_{res}C}} \quad (9)$$

The power losses in the damping resistor will be

$$\boldsymbol{P_{loss} = 3 \times R_d} \quad (10)$$

where h is the harmonic order of the current flowing through Rd. In the LCL filter-based DSTATCOM topology, Rd is chosen such that the damping losses are minimized while assuring that the sufficient resonance damping is provided to the system. The reason for considering damping power losses is that the significant current is drawn by the shunt part of the LCL filter. This further reduces the efficiency of the VSI. However, one of the major advantages of the proposed scheme is that the voltage across, and therefore the current through the shunt part of the LCL filter, is greatly reduced. This reduction in the shunt current significantly reduces the damping power losses. Therefore, sufficient resonance damping of the system is a prime concern while designing a damping resistor in the proposed method. For C = 10 μF and fres = 2400 Hz, the reactance offered by C at fres is 6.63 Ω. Here, a 15-

Ω resistance is chosen, which provides satisfactory resonance damping. 3) Design of Series Capacitor Cse: The main criterion for designing of Cse is that it should provide a low impedance path for the fundamental frequency current component [17]. It was ensured that the shunt capacitor C will provide a high impedance path for the lower order harmonics. Therefore, a negligible fundamental current will be drawn by C and can be neglected at the fundamental frequency. Therefore, the fundamental current supplied by the filter while considering R1, L1, R2, L2, and Cse as series connected is given as

$$\boldsymbol{I_f^1 = \frac{V_{inv1} - V_{t1}}{R_f + j(X_{f12} - X_{sc1})}} \qquad (11)$$

where Rf = R1 + R2, Xf12 = ω1(L1 + L2), Xse1 = 1ω1Cse, and Vt1 is the fundamental rms PCC voltage. The voltage Vinv1 is the fundamental rms voltage per phase available at the VSI terminal and is given as [29]

$$\boldsymbol{V_{inv1} = \frac{V_{dc}}{\sqrt{2}}} \qquad (12)$$

After simplification, (11) becomes

$$\boldsymbol{I_f^1 = \frac{(V_{inv1} - V_{t1})R_f - j(V_{inV1} - V_{t1})(X_{f12} - X_{sc1})}{R_f^2 + (X_{f12} - X_{sc1})^2}} \qquad (13)$$

Interfacing resistances are very small compared with reactive part and can be neglected. Therefore, the imaginary part magnitude of **I**1f will be

$$\boldsymbol{. I_m\left(I_f^1\right) = -\frac{V_{inv1} - v_{t1}}{X_{f12} - X_{sc1}}} \qquad (14)$$

It can be observed from (14) that to inject reactive current from the compensator to the PCC, the fundamental rms voltage per phase available at the VSI terminal (i.e., dc-link voltage) must be much greater than the terminal voltage. Otherwise, the compensation performance will not be satisfactory. In the traditional topology where the series capacitor is absent, the maximum injected current only depends upon the dc-link voltage (since Vt1 and Xf12 are fixed). Therefore, the dc voltage is maintained at a much higher value as compared with the terminal voltage. Insertion of the capacitor in series with the interfacing LCL filter results in the reduction of the total impedance provided by the compensator, which is also evident from (14). Therefore, the dc-link voltage can be reduced from its reference value for the same reactive current injection. Hence, the value of the series capacitor depends upon the maximum reactive filter current and to the extent that the decrease in the dc-link voltage is required. The maximum reactive current that a compensator can supply must be the same as that of the maximum load reactive current to achieve unity power factor at the load terminal. The load current will be maximum when it will offer minimum impedance (Zlmin = Rlmin + jXlmin), i.e., at full load. Therefore, the maximum fundamental current drawn by the load in a particular phase is given as

$$\boldsymbol{. I_{lmax} = \frac{V_{t1}}{R_{lmin} + jX_{lmin}}} \qquad (15)$$

Calculating the imaginary load current magnitude from the preceding equation and equating with (14)

$$. \frac{V_{t1}X_{lmin}}{Z_{lmin}^2} = \frac{V_{inv1} - V_{t1}}{X_{f12} - X_{sc1}} \qquad (16)$$

A more generalized expression can be written as

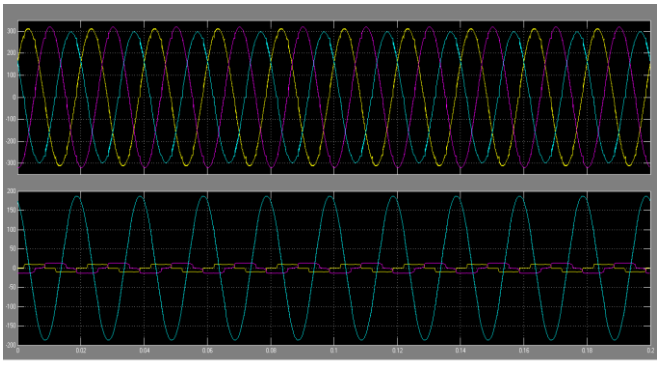
$$I_{lmax}\sqrt{1 - pf_{lmin}^2} = \frac{V_{inv1} - V_{t1}}{X_{f12} - X_{sc1}} \qquad (17)$$

where Ilmax = Vt1/Zlmin, and pflmin is the minimum loadpower factor given by Rlmin/Zlmin. Hence, Xse1 will be.

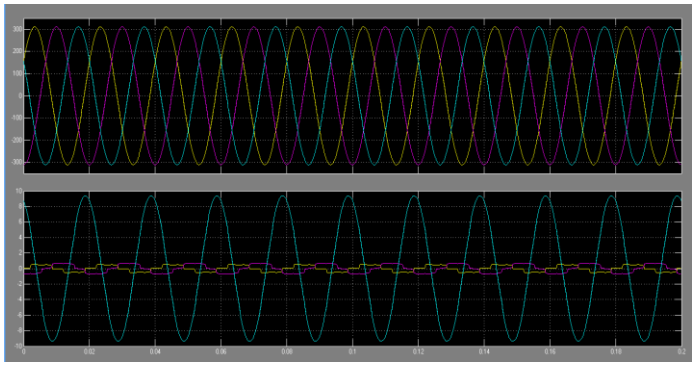
$$X_{sc1} = X_{f12} - \frac{V_{inv1} - V_{t1}}{I_{lmax}\sqrt{1 - pf_{lmin}^2}} \qquad (18)$$

TABLE I SIMULATION PARAMETERS

System quantities	Values
Source voltage	230 V rms line to neutral,50 HZ
Fedder impedence	Z_s =1+j3.14Ω
Linear load	Z_{la} =30 + j62.8 Ω Z_{lb} =40 + j78.5 Ω, Z_{lc} =50 + j50.24 Ω
RC type non linear load	R1 = 50Ω C1 = 1000μF
Rl type non linear load	R1 = 50 Ω L1 = 200 mH
Hysteresis band	± 0.5A



(a)



(b)

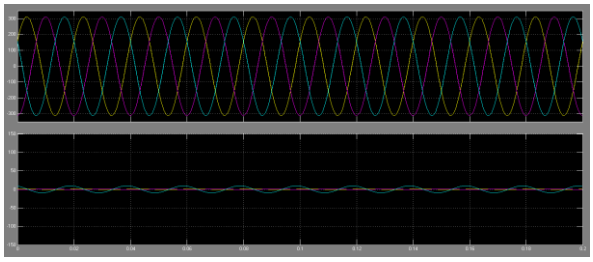
Fig.4. simulation result without compensation. (a) Source currents. (b) PCC voltage

We can use (16) when the load impedances are known, whereas in practical situations, only nameplate data are available, and thus, (18) should be used. Based on the values given in Table I, where phase-b requires the maximum reactive current having the minimum impedance, the value of the series capacitor can be computed. For the given values, Cse is found to be 46.13 μF. For practical considerations, Cse is taken as 50 μF.

V. SIMULATION RESULTS

The advantages of the proposed topology are that it uses a lower rating of the VSI, has a smaller value of the filter inductor, reduces the damping power loss, and provides improved current compensation. All these advantages are verified through PSCAD software. System parameters used to validate the performance are given in Table I. Fig. 4(a) shows the threephase source currents before compensation which are same as load currents. These currents are unbalanced and distorted due to presence of unbalanced linear and nonlinear loads. Three- phase PCC voltages, as shown in Fig. 4(b), are unbalanced and distorted due to presence of feeder impedance. The performance of the traditional DSTATCOM topology is presented in Fig. 5. The three-phase source currents, which are balanced and sinusoidal, are shown in Fig. 5(a). Fig. 5(b) shows the three-phase PCC voltages. As seen from waveforms, both the source currents and the PCC voltages contain switching frequency components of the VSI. The three-phase filter currents are shown in Fig. 5(c). The waveforms of voltages across upper and lower dc capacitors, as well as the total dc-link voltage, are presented in Fig. 5(d). The voltage across each capacitor is maintained at 520 V, whereas the total dc-link voltage is maintained at 1040 V using the PI controller. Fig. 6 shows the compensation performance for LCL filterbased DSTATCOM. The source currents and PCC voltages are balanced and sinusoidal but contain significant switching harmonics ripple. Their percentage total harmonic distortions (THDs) are given in Table II. To accommodate power losses in the damping resistor, the source currents are slightly increased compared with the traditional topology. Moreover, the total dc-link voltage is maintained at 1040 V (same as the traditional scheme) to achieve load compensation. The compensation performance of the proposed topology is shown in Fig. 7. The load and source parameters are the same as given in Table I. In Fig. 7(a), the three-phase source current waveforms are shown, which are balanced, sinusoidal, and have negligible switching ripple compared with the traditional topology. In addition, neutral current is nearly zero. Fig. 7(b) shows the three-phase compensated PCC voltages with reduced switching harmonics. Additionally, source currents are in phase with their respective phase voltages. The filter currents, as shown in Fig. 7(c), have smaller ripples as compared with that of the traditional topology. The voltages across each capacitor and the total dc-link voltage are shown in Fig. 7(d), having maintained at 110 and 220 V, respectively. The performance of the proposed topology is compared with traditional DSTATCOM topologies, and

corresponding percentage THDs in voltages and currents are illustrated in Table II. It is clear from Table II that the percentage THDs in three-phase source currents and in PCC voltages are considerably lesser in the proposed topology. Moreover, these confirm that the reduced dc-link voltage is sufficient for the DSTATCOM to achieve its current compensation performance. Comparative analysis of VSI parameters in terms of dc-link voltage, total filter inductance, and energy stored in passive components is presented in Table III. Furthermore, the performance of the proposed topology with the RC-type nonlinear load is shown in Fig. 8. The source currents are sinusoidal with a negligible harmonic component, although load currents are highly distorted. The PCC voltages are also balanced and sinusoidal with a small ripple component. Again, the total dc-link voltage is maintained at 220 V (110 V across each capacitor). This confirms that the reduced dc-link voltage is sufficient to compensate the RC-type nonlinear load effectively.



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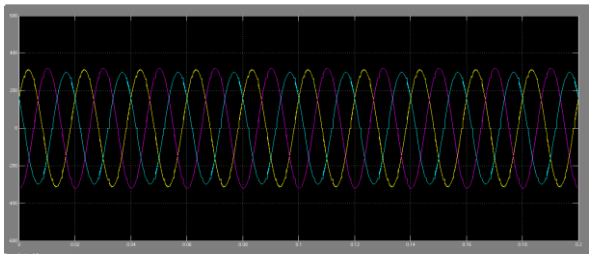

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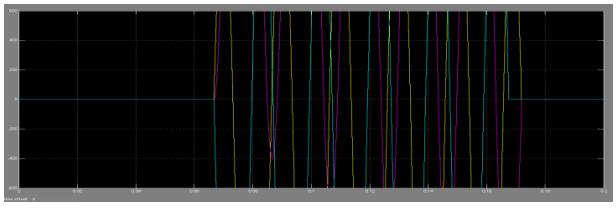

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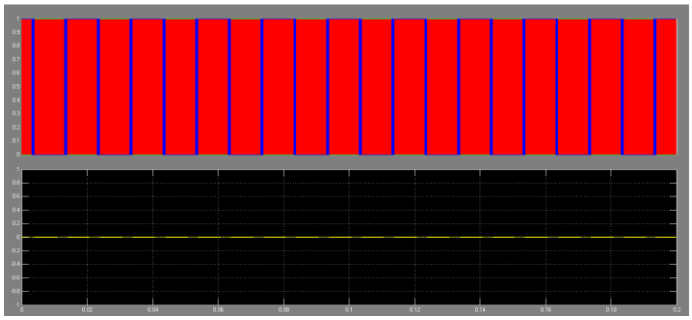
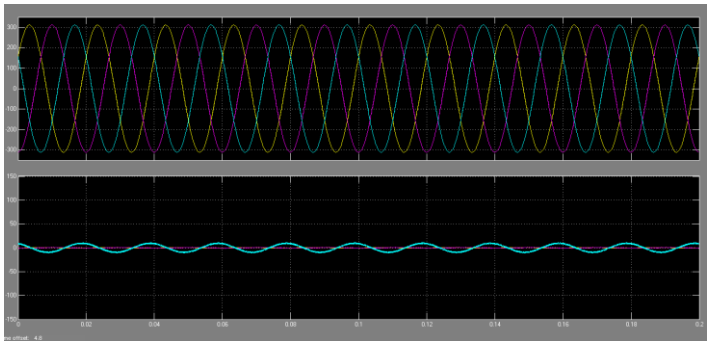
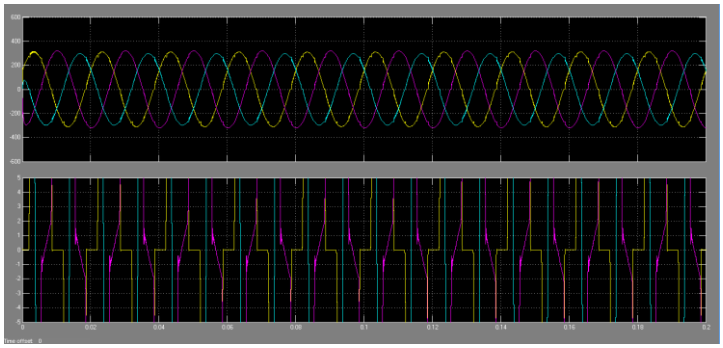


(d)

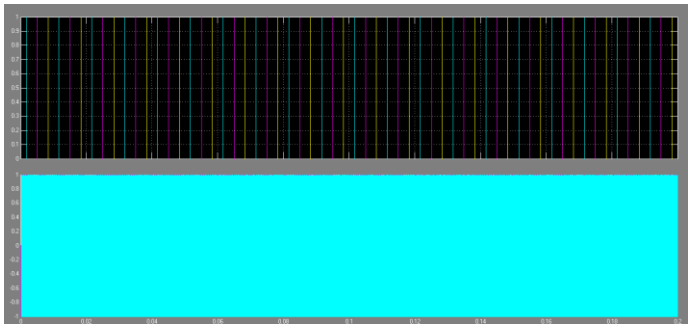
Fig. 5. Simulation results for traditional topology. (a) Source currents. (b) PCC voltages. (c) Filter currents. (d) Voltages across the dc link.



(a)



(b)



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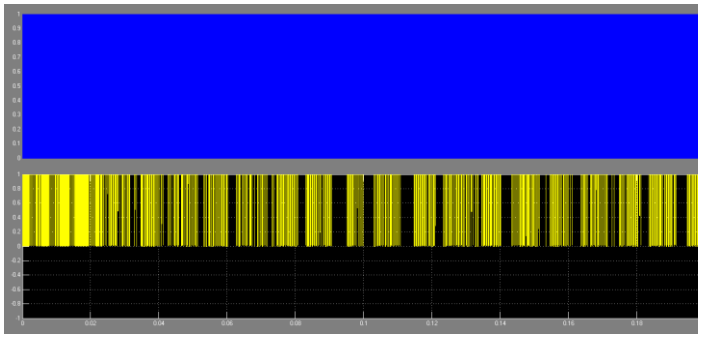

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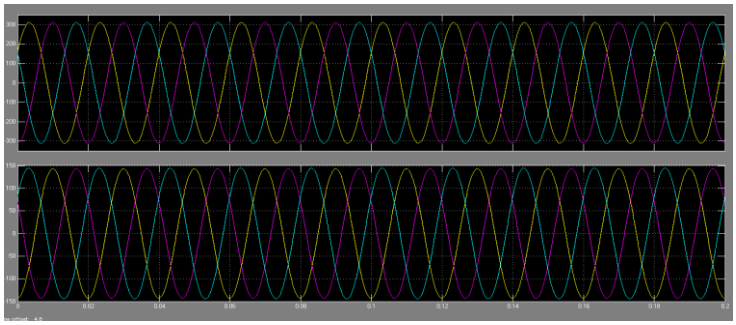
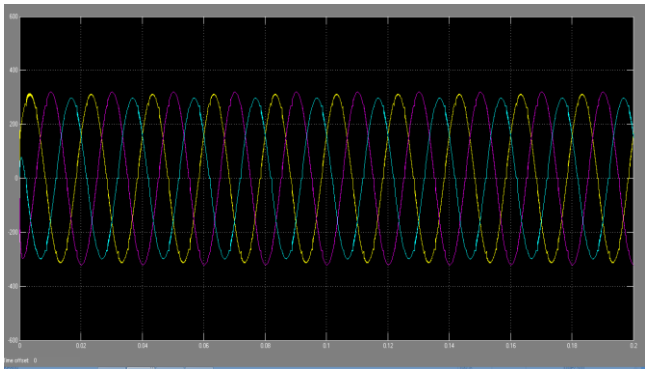


(a)

Fig.6. simulation results for DSTACOM with the LCL filter. (a) Source current. (b) PCC voltages. (c) Filter currents. (d) Voltage across the dc link.



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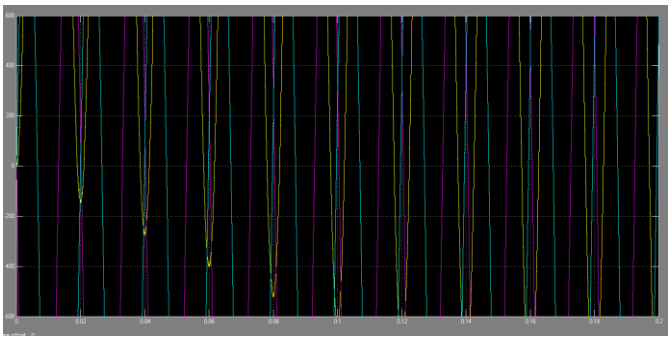

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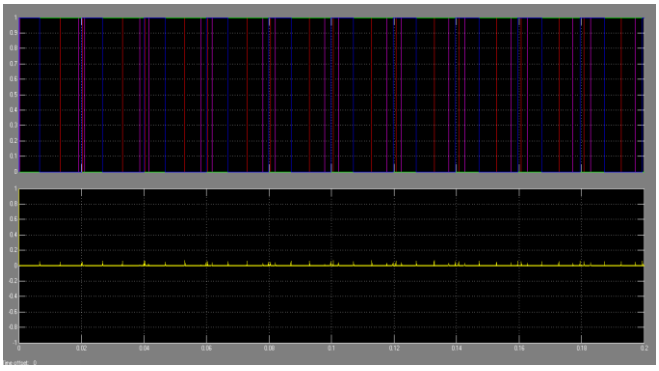


(d)

Fig.7. Simulation results for the proposed topology. (a) Source current. (b) PCC voltages. (c) Filter currents. (d) Voltage across the dc link

A. Reduction in the VSI Power Rating

The power rating of DSTATCOM, i.e., SC, is given as [9]

$$S_C = \sqrt{3}\frac{V_{dc}}{\sqrt{2}} I_{f1} \qquad (19)$$

The dc bus voltage requirement has been decreased from 520 to 110 V. The term If1 represents the rms current supplied by the IGBT switch. In the traditional DSTATCOM topology, the rms value of If1 will be the same as that of the rms reactive and harmonics component of the load current. In the following section, it can be seen that the current drawn by the shunt branch of the LCL filter is not much. Hence, the current rating of the IGBT switch in both topologies will be approximately the same. Therefore, the ratio of the power rating of the proposed topology SCP to the traditional topology SCT will be

$$\frac{S_{CP}}{S_{CT}} = \frac{110}{520} = 0.2115 \qquad (20)$$

The power rating of the proposed topology will be only 21.15% of the traditional topology. The reduction in size of passive components and power rating will result in higher efficiency, less switching ripple, and electromagnetic emissions. Moreover, the current through the shunt capacitor in the proposed topology is reduced compared with the LCL filter-based DSTATCOM topology. It further reduces the power rating of the proposed topology as compared with the LCL filter-based DSTATCOM.

B. Reduction in Damping Power Loss and Effects

Passive damping is easy to implement and provides good resonance elimination capability; this also results in extra power loss in the damping resistor. However, in industrial applications

TABLE II PERCENTAGE THDS IN SOURCE CURRENTS AND PCC VOLTAGES

System configuration	i_{sa}	i_{sb}	i_{sc}	v_{ta}	v_{tb}	v_{tc}
Without compensation	15.43	15.18	14.18	12.41	12.21	12.33
Compensation with traditional topology	1.68	1.60	1.67	4.52	3.92	4.70
Compensation with LCL filter	0.32	0.30	0.36	0.85	0.76	0.88
compensation with proposed topology	0.17	0.13	0.13	0,41	0.45	0.44

TABLE III COMPARISON OF VSI PARAMETERS

DSTATCOM topology	Inductor value	Voltage at DC link	Energy stored in passive components
Traditional	26 mH	1040V	811.2 J
With LCL filter	7.5 mH	1040 V	811.2 J
Proposed	2.1 mH	220 V	36.3 J

where the requirements are to have the minimum number of sensors with the least complex algorithm, passive damping is preferred while accepting the power loss [22]. The current through the damping resistor depends upon the voltage across the shunt part of the LCL filter. In the proposed scheme, the dc-link voltage has been greatly reduced. Therefore, the voltage at the shunt part of the LCL filter will alsoreduce considerably. It will reduce the current flowing through the damping resistor and, therefore, damping power as well. Fig. 9(a) shows the filter current in phase-a when only LCL filter-based DSTATCOM is used. The steady-state rms value of current in the damping resistor is found to be 4.5 A. The power loss in the damping resistor is obtained as follows:

$$\mathbf{P_{loss1} = 3 \times R_d \times I_{sh}^2 = 3 \times 4.5^2 \times 15 = 911.25W} \quad (21)$$

Fig. 9(b) shows the current through the damping resistor in the proposed DSTATCOM topology. The effect of reduced dc-link voltage (110 V in this case) can be clearly seen from the steady-state rms damping current, which is reduced to 1.05 A. The power loss can be computed as follows:

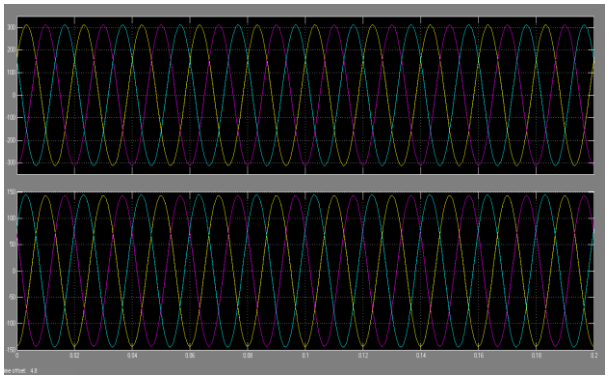
$$\mathbf{P_{loss2} = 3 \times 1,05^2 \times 15 = 48.61} \quad (22)$$

The damping resistor power loss ratio of the proposed DSTATCOM topology and the DSTATCOM with only the LCL filter can be calculated as follows:

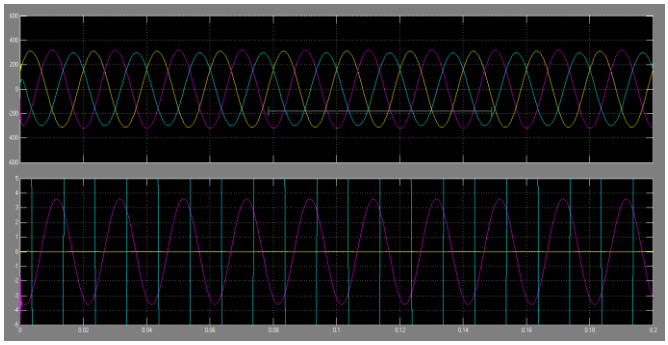
$$\frac{\mathbf{P_{loss1}}}{\mathbf{P_{loss2}}} = \frac{\mathbf{48.61}}{\mathbf{911.25}} = \mathbf{0.0533}$$

The damping power loss in the proposed topology is only 5.33% as compared with the DSTATCOM employing the LCL filter. It results in higher efficiency of the VSI. The decrease in shunt capacitor current causes the decrease in the current supplied by the VSI. Therefore, the loss in the VSI and the reactive power losses in the shunt capacitor and L1 will decrease. Damping power loss is compensated by drawing real power from the source. Reduction in damping loss ensures that the source currents are also reduced. Finally, the dynamic performance of the proposed scheme is tested by varying the load power demand at t = 1.5 s. Fig. 10(a)–(e) shows source currents, load currents, filter currents, dc-link voltages, and load powers, respectively. The source currents are balanced and sinusoidal during the entire operation, except the initial transients during load change. During load change, the dc-link voltage deviates from the reference value. However, the PI controller brings back the dc-link voltage at its reference voltage.

These results confirm the ability of the proposed scheme to operate in dynamic load conditions.



(a)



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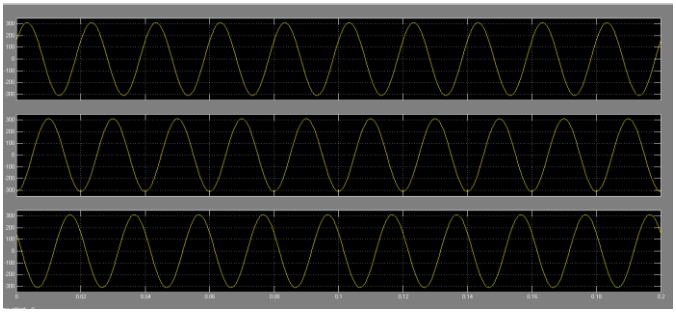

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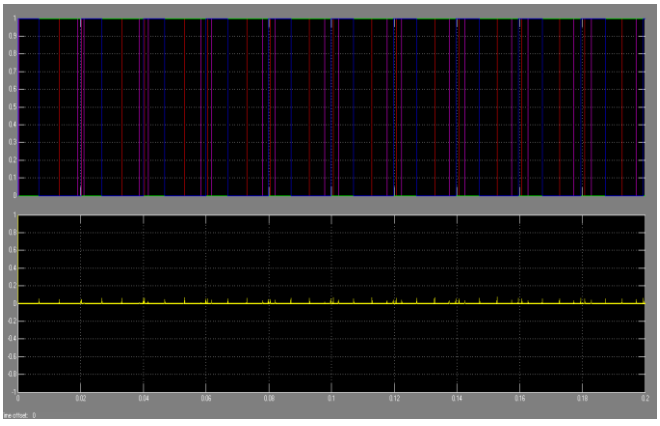

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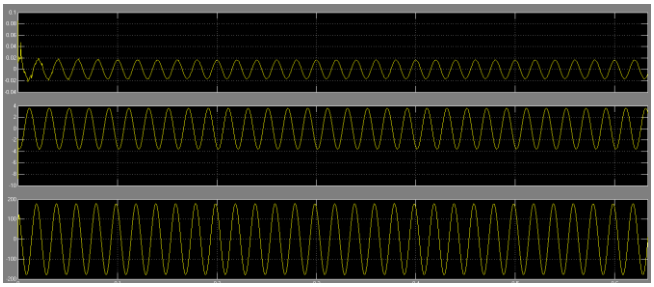

(e)

Fig.8. simulation results for the proposed topology with the RC –type nonlinear load. (a) Source current. (b) PCC voltages. (d) Voltages across the dc link. (e) Load currents.

VII. CONCLUSION

In this paper, design and operation of an improved hybrid DSTATCOM topology is proposed to compensate reactive and harmonics loads. The hybrid interfacing filter used here consists of an LCL filter followed by a series capacitor. This topology provides improved load current compensation capabilities while using reduced dc-link voltage and interfacing filter inductance. Moreover, the current through the shunt capacitor and the damping power losses are significantly reduced compared with the LCL filter-based DSTATCOM topology. These contribute significant reduction in cost, weight, size, and power rating of the traditional DSTATCOM topology. Effectiveness of the proposed topology has been validated through extensive computer simulations and experimental studies.

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