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Fast and Approximate Processing Unit for 2D Discrete Cosine System

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Abstract
The recent time witnesses a tremendous need for high performance digital signal Processing (DSP) systems for high end emerging applications like HD-TV, medical imaging, satellite communication, 3G mobile technologies etc. For all these applications, the sources of data are video signals. For transmission of video signals significant amount of bandwidth required. Since the captured video data contain huge amount of redundant data, there is an opportunity for video data compression keeping the picture quality intact. DCT is a well known technique used in video or image compression. DCT algorithms are computation intensive and involve large number of multiplication and addition operations. Therefore, with the increase in number of length of the DCT,the number of multiplication and addition operations also increase leading to larger chip area and performance degradation. The primary aspect of the 2-D DCT computation is to compute the DCT coefficients, where a large number of mathematical computations are required. This work is implemented on Matlab and hardware level by using of Verilog hardware language. Many researchers provided different architectures targeting area or speed or throughput with non scalable approach for computation.

1. INTRODUCTION

In classical lossy image compression techniques where transform coding is used, the transform is applied to non-overlapping sub-blocks of the image. This is in particular the case with the lossy modes of JPEG, where a 2D discrete cosine transform (DCT) is applied to non-overlapping 8 * 8 sub-blocks. Yet it is standard practice to use windowed overlap-and-add transforms, specifically the windowed modified DCT (MDCT), in audio compression techniques. The reason for doing so is to mitigate undesirable edge effects, namely the contamination of frequency components caused by the resulting discontinuities at the boundaries of transform blocks.

While modern transform coding based image compression algorithms (such as JPEG2000) have eliminated this problem by applying wavelet transforms to entire images, one is still faced with the question: What if we were to do the same in image compression as is done in audio compression, replacing the standard DCT with a windowed MDCT?

MDCT is one of the core units in JPEG XR which consumes more time in compression unit. Apart from this the previous works are mainly focused on accurate analysis and efficient estimations of frequency of advance audio applications. There is no efficient and swift unit for MDCT in JPEG XR. The main theme of the work is to minimize the simulation time for a compressor unit using the bit depth of the image with a scalable coefficients with a varying cost of quality of Image. For optimal quantization we adapt and apply an algorithm, designed for JPEG, to MJPEG.

Imaging and video applications are one of the fastest growing sectors of the market today. Typical application areas include e.g. medical

imaging, HDTV, digital cameras, set-top boxes, and machine vision and security surveillance. As the evolution in these applications progresses, the demands for technology innovations tend to grow rapidly over the years. Driven by the consumer electronics market, new emerging standards along with increasing requirements on system performance imposes great challenges on today's imaging and video product development. To meet with the constantly improved system performance measured in, e.g., resolution, throughput, robustness, power consumption and digital convergence (where a wide range of terminal devices must process multimedia data streams including video, audio, GPS, cellular, etc.), ne design methodologies and hardware accelerator architectures are constantly called for in the hardware implementation of such systems with real-time p An image scaling is applied when variable size images are delivered to users from different multimedia sources such as mobile phone, digital camera, and Internet. When the resolution of the received image is low, the user needs to magnify the image and display it via the high resolution display devices. However, resizing the image would produce severe jagging and blurring in the HR image. For example, a video source with a 640× 480 video graphics array resolution may need to fit the 1920×1080 resolution of a high-definition multimedia interface, this is achieved my means of image scaling processor. It has become a significant trend to design a low-cost, high quality, and high performance image scalar by VLSI technique for multimedia electric products.

IMAGE scaling is widely used in many fields ranging from consumer electronics to medical imaging. It is indispensable when the resolution of an image generated by a source device is different from the screen resolution of a target display. For example, we have to enlarge images to fit HDTV or to scale them down to fit the mini-size portable LCD panel. The most simple and widely used scaling methods are the nearest neighbor and bilinear techniques. According to the required computations and memory space, we can divide the existing scaling methods into two classes: lower complexity and higher complexity scaling techniques. The complexity of the former is very low and comparable to conventional bilinear method.

2. LITERATURE REVIEW

As the technology changing the use of compression is more and demanding still the efficient process of reducing the size. As we see DCT is the core computational block in image compression , where DCT is used to transform the data into frequency domain many researchers have provided different approach to reduce simulation time or memory efficiency or both at both software and hardware level. The below various researchers provide their approach,

1. Yuebing Jiang; Pattichis, M.,(2012),[9] In this paper, we studied the dynamically reconfigurable DCT architecture system that can be used to optimize performance objectives subject to real-time constraints on power, image quality, and bitrate. The proposed system is validated on the LIVE image database for maximum image quality, minimum power, minimum bitrate, and typical modes.
2. Jin Zeng; Au, O.C.; Wei Dai; Yue Kong; Luheng Jia; Wenjing Zhu,(2013),[1] In this paper, an overview of existing image and video compression standards is presented. As for image coding standards, JPEG and JPEG 2000 are introduced and the comparison is given to show that both standards have their own advantages and enjoy popularity under certain circumstances. In addition, a brief discussion about MPEG-1, MPEG-2, MPEG-4, H.261, H.263, H.264/MPEG-4 AVC and HEVC is included to provide a review of video coding standards and their key features and applications.
3. Strang, Gilbert,(1999),[4], The success of any transform in image coding depends on a combination of properties |mathematical, computational, and visual. The relation to

the human visual system is decided above all by experience. This article was devoted to the mathematical property of orthogonality (which helps the computations). There is no absolute restriction to second di_erence matrices, or to these very simple boundary conditions.

4. Park, Jongsun, Soonkeon Kwon, and Kaushik Roy,(2002), [8],In this paper present a DCT architecture based on computation sharing multiplier (CSHM) , which specifically targets computation re-use in DCT matrix multiplication. it also propose a reconfigurable DCT architecture for low power. Using the CSHM algorithm, the DCT matrix multiplication can be significantly simplified to add and shift operations of alphabets multiplied by input x. The idea presented in this paper can assist design of DSP algorithms and their implementation for low power application.
5. Yuebing Jiang; Pattichis, M, (2012),[9], In this paper, represent a dynamically reconfigurable DCT architecture system that can be used to maximize image quality while meeting real-time constraints on bitrate and dynamic power. Optimal DCT architectures are computed off-line and implemented in real-time using dynamic partial reconfiguration.
6. Yuebing Jiang; Pattichis, M (2012), [10]In this paper, studied a dynamically reconfigurable DCT architecture system that can be used to optimize performance objectives subject to real-time constraints on power, image quality, and bitrate. The proposed system is validated on the LIVE image database for maximum image quality, minimum power, minimum bitrate, and typical modes.
7. Jongsun Park; Jung-Hwan Choi; Roy, K., (2010), [11] ,In this work, propose a low power, reconfigurable DCT architecture to allow efficient tradeoff between image quality and computation energy. The DCT architecture uses the dynamic bit-width adaptation, where operand bit-widths are changed according to image quality and/or power consumption requirements. Different tradeoff levels are specified and the proposed DCT architecture can be dynamically reconfigured from one tradeoff level to another.
8. Wei Zheng; Yanchang Liu,(2011), [12], Application of binary DCT is presented in this paper, which is a fast DCT algorithm with lifting scheme. The complexity of binary DCT are reduced, comparing with existing algorithm as its multiplierless. Moreover, binary DCT is implemented based on public JPEG encoder and its performance achieve the same level as public JPEG standard. At last but not least, binary DCT can be implemented with 16-bit data bus, making it very suitable for low-lost, fast and low-power multimedia applications.
9. Karakonstantis, G.; Banerjee, N.; Roy K.(2010), [19] In this paper the DCT architecture that simultaneously satisfies low-energy requirements and tolerance to process variations while maintaining a reasonable PSNR for image compression. This is achieved by making the high-energy computational paths faster compared to their low-energy counterparts using both circuit and algorithm-level techniques, and making sure that maximal sharing of logic is achieved. the proposed architecture is that it predicts and tolerates any path delay failures in longer paths under process variations, thereby maintaining high image quality.

PROPOSED METHODOLOGY

The following is a general overview of the JPEG process. The proposed algorithm is as mentioned:

1) The input image can be read by using imread function and then broken into 8x8 block of matrixes.
2) The algorithm can be applied for gray scale by suitably using functions such as is gray

functions.

3) DCT is applied to each block on its both the rows and columns. Strassen's matrix multiplication algorithm is applied on the DCT matrix multiplication calculation.
4) Each block is compressed by quantization. Suitably the quantization matrix is selected. They are standard matrices used in JPEG.
5) The array of compression blocks that constitute the image is stored in a significantly reduced amount of space.
6) The image is reconstructed through decompression using Inverse DCT.

Fig 3.1:- lena images of different- different block size

4. IMPLEMENTATION:

4.1 Image analysis for Energy distribution:

Some of the standard images are taken to calculate the energy distribution (Frequency analysis). As per the energy distribution we can find the minimum number of pixel required to compute as per the human vision.

One important point in JPEG block is quantization. Quantization, included in picture handling, is a lossy pressure procedure accomplished by packing a scope of qualities to a solitary quantum esteem. At the point when the quantity of discrete images in a given stream is diminished, the stream turns out to be more compressible

A run of the mill JPEG codec meets expectations by breaking the photo into discrete hinders (8×8 pixels).These squares can then be subjected to discrete cosine change (DCT) to compute the recurrence segments, both on a level plane and vertically. The subsequent piece (the same size as the first square) is then premultiplied by the quantization scale code and partitioned component insightful by the quantization grid, and adjusting every resultant component. The quantization lattice is intended to give more determination to more distinguishable recurrence segments over less noticeable parts (typically lower frequencies over high frequencies) notwithstanding changing the same number of segments to 0, which can be encoded with most prominent effectiveness

A common quantization matrix is:

$$\begin{bmatrix} 16 & 11 & 10 & 16 & 24 & 40 & 51 & 61 \\ 12 & 12 & 14 & 19 & 26 & 58 & 60 & 55 \\ 14 & 13 & 16 & 24 & 40 & 57 & 69 & 56 \\ 14 & 17 & 22 & 29 & 51 & 87 & 80 & 62 \\ 18 & 22 & 37 & 56 & 68 & 109 & 103 & 77 \\ 24 & 35 & 55 & 64 & 81 & 104 & 113 & 92 \\ 49 & 64 & 78 & 87 & 103 & 121 & 120 & 101 \\ 72 & 92 & 95 & 98 & 112 & 100 & 103 & 99 \end{bmatrix}$$

Dividing the DCT coefficient matrix element-wise with this quantization matrix, and rounding to integers results in:

$$\begin{bmatrix} -26 & -3 & -6 & 2 & 2 & -1 & 0 & 0 \\ 0 & -3 & 4 & 1 & 1 & 0 & 0 & 0 \\ -3 & 1 & 5 & -1 & -1 & 0 & 0 & 0 \\ -4 & 1 & 2 & -1 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

For example, using −415 (the DC coefficient) and rounding to the nearest integer

$$\operatorname{round}\left(\frac{-415}{16}\right) = \operatorname{round}(-25.9375) = -26$$

From above quantized matrix we see that most of the pixel values are near to zero or zero which does not have any energy having with it. So from the test image we see a graph as shown below where the most of energy lies in the first 20-25 pixel. So by selecting only the first energy pixel one can easily reduce the simulation time

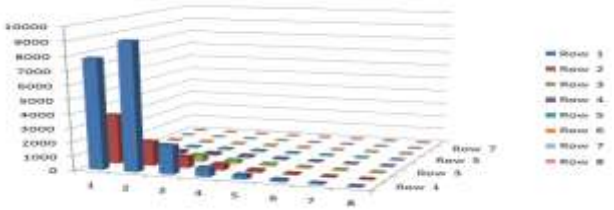


Fig 4.1.1:- Energy distribution graph of 64 coefficient of image & it shows only 20-25 coefficient contain more information for generate original image

The graph suggest that most of the energy is surrounded in lower frequency corner specifically first 20 coefficient (in zig-zag manner) contains more than 85+% of energy. Based on energy

distribution of image after 2D DCT which demonstrates that few low frequency components (top corner shown in Fig) are capable of representing the entire image, with minute quality degradation. This can be helpful in realization of approximate architecture. Instead of computing complete 8x8 block, the proposed architecture computes only first 20-25 coefficients generated (5x5 matrix's) using matrix multiplication rule and significant computations. As an outcome of matrix multiplication, fewer coefficients are required to process from input end.

Our contributions are as follows:

• Based on Energy Distribution for 2D-DCT, 20-25 coefficient DCT structure is realized.

Fig 4.1.2:-The above figure shows the standard Lena image extracted at every pixel value.

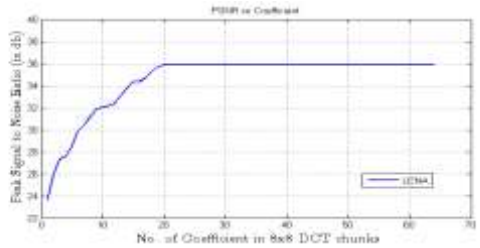


Fig 4.1..3:- The above figure shows the coefficient-wise distribution of PSNR responsible for Image quality assessment.

Minimum PSNR regarded for good viewing is 25 db. The graph becomes constant after 20 coefficients and further improvement is unnoticeable.

In similar way we extracted all the analysis of images for every parameter.

4.2 Error resilient DCT Implementation for Hardware approach.

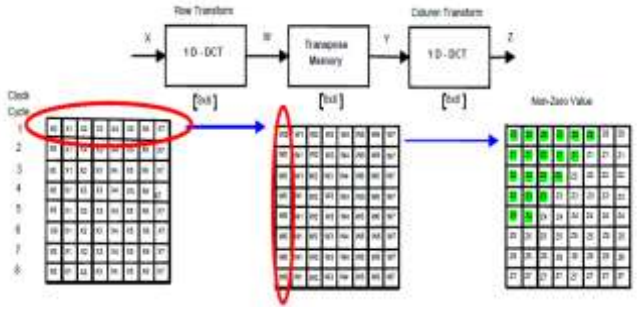


Fig 4.2.1:- figure shows convolution of 8*8 1D-DCT & memory, output is non zero values.

Design strategy for 20 coefficient design structure: on the basis of Matrix Multiplication, shown figure. This has evolved as the reverse engineering Approach going backward to cross two 1D-DCT to make it designed for 20 coefficient generation.

4.2.1 Advantages of the Design

1. Reduction in Complexity:- By this Some coefficient (like lower 3 value) are not necessary to contribute to the design hence they are avoided to compute and in return hardware complexity is reduced.
2. Total Computation Time Reduction (analytical approach)

4.3 Our approach:-

1st DCT= 5x8 in dimension

Reduction in coefficient as 64-40 = 24

2nd DCT = 5x4

Reduction in coefficient as 64-20 = 44

There is a saving in time.

Comparison of Data size

Image	20 coef. size	Original size	Compression(%)
lena	126kb	151kb	16.55
barbara	145kb	182kb	20.32
boat	136kb	174kb	21.83
couple	134kb	190kb	29.47
hill	133kb	206kb	35.43
man	140kb	205kb	31.70
flinstones	168kb	171kb	1.75
fingerprint	180kb	181kb	0.55

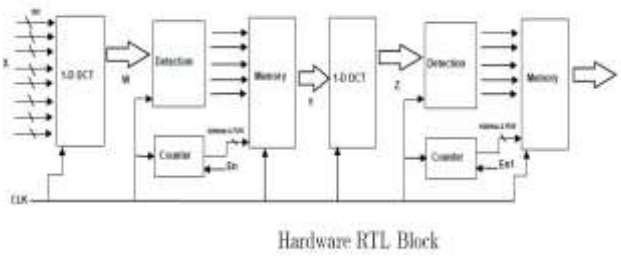
• Data Compression:

$$Compression = (1 - \frac{\text{Size obtained from First 20 coefficient image}}{\text{original size image}}) * 100\%$$

Table 4.3.1:- shows the percentages of compression is increased in different images with taking only 20 coefficient.

4.4. FPGA implementation

• For the implementation in FPGA, the algorithm is coded in the verilog Xilinx vertex 4



Hardware RTL Block

Fig 4.4.1:-figure shows the block diagram of FPGA hardware Implementation.

The input is processed first by 1D-DCT and the negative terms are detected & stored in memory and again for 2nd Dimension DCT, the memory is fetched processed with signed of input to the block and again stored in memory.

4.3.1 Stassen's matrix multiplication algorithm:

The standard method of matrix multiplication of two n × n matrices takes O(n3) operations. Stassen's algorithm is a Divide-and-Conquer algorithm that is asymptotically faster. The usual multiplication of two 2 × 2 matrices takes 8 multiplications and 4 additions. Strassen's shows how two 2 × 2 matrices can be multiplied using only 7 multiplications and 18 additions. If we Imagine that A and B are each partitioned into four square Strassen showed that 2x2 matrix multiplication can be accomplished in 7 multiplication and 18 additions or subtractions. (2log27 =22.807)

Stassen's algorithm

• Partition A, B and and C into 4 equal parts:

$$C = \begin{bmatrix} C11 & C12 \\ C21 & C22 \end{bmatrix} \qquad A = \begin{bmatrix} A11 & A12 \\ A21 & A22 \end{bmatrix}$$

• Evaluate the intermediate matrices

$$M1 = (A11 + A22)(B11 + B22)$$
$$M2 = (A21 + A22) B11$$
$$M3 = A11 (B12 - B22)$$
$$M4 = A22 (B21 - B11)$$
$$M5 = (A11 + A12) B22$$
$$M6 = (A21 - A11)(B11 + B12)$$
$$M7 = (A12 - A22)(B21 + B22)$$

• Construct C using the intermediate Matrices:

$$C11 = M1 + M4 - M5 + M7$$
$$C12 = M3 + M5$$
$$C21 = M2 + M4$$
$$C22 = M1 - M2 + M3 + M6$$

Description of Algorithm:

• Partition A and B into quarter matrices as described above.

• Compute the intermediate matrices:

- If the sizes of the matrices are greater than a threshold value, multiply the Recursively using Stassen's algorithm.
- Else use the traditional matrix multiplication algorithm.

• Construct C using the intermediate matrices.

5. RESULT & ANALYSIS

5.1. Performance Evaluation Parameters

Various parameters are used to evaluate the proposed algorithm at both levels. The various parameters are

1. PSNR (Peak signal-to-noise ratio)
2. SSIM (structural-similarity-based image quality assessment)
3. FSIM (Feature Similarity Index for Image Quality Assessment)
4. Gradient Magnitude Similarity deviation (GMSD)
5. Riesz-transform based Feature Similarity metric (RFSIM)

5.2. Results of Image analysis:

1. Absolute difference

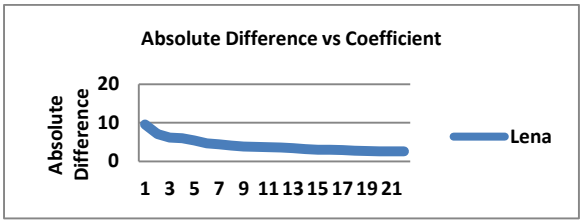


Fig 5.2.1:- figure shows graph of absolute difference vs Coefficient

In this graph we shows that the if we generate the original image by taking the coefficient of 1,6,11,16,21,26….etc. then original image are absolutely differed on following terms which shown in graph. Now we can see that absolute difference is reached to approximate zero with taking only coefficient of 21-26.

2. Correlation

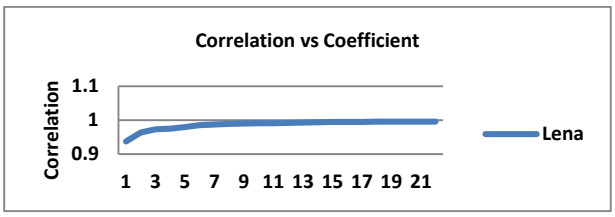


Fig 5.2.2:- figure shows graph of correlation vs coefficient

In this graph we shows that the correlation between original image and generated image is very less and it's reached to label 1 for only 19-25 coefficient.

3. FSIM (Feature Similarity Index for Image Quality Assessment):- The analysis of FSIM is of two stages, in the first stage, the local similarity map is processed and computed, and then in the next stage, it pools the similarity mapped to compute into a single similarity score. The separation of the feature similarity measurement between f1(x) and f2(x) into two components, each for PC or GM is same. Initially the similarity measure for PC1(x) and PC2(x).

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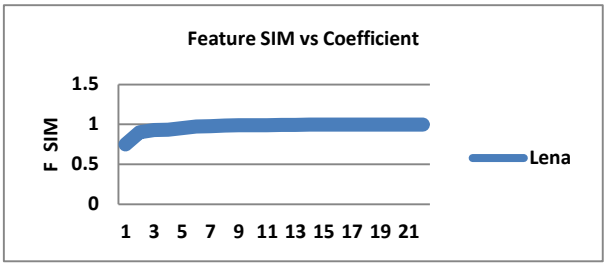

Fig 5.2.3- figure shows the graph of Feature SIM vs Coefficient

In this graph we shows that the feature SIM evaluation parameter are obtaion 1 and above in the coefficient of 11-21.then we can say that only 20-25 coefficient can provide good FSIM parameter value.

4. GMSD (Gradient Magnitude Similarity Deviation) :- For digital images, the gradient magnitude is defined as the root mean square of image directional gradients along two orthogonal directions. The gradient is usually processed and computed by multiplying an image with a linear filter such as the classic Roberts, Sobel, Scharr and Prewitt filters and some task-specific ones. For simplicity of computation and to introduce a modicum of noise-insensitivity, we utilize the Prewitt filter to calculate the gradient because it is the simplest one among the 3×3 template gradient filters. Other filters such as Sobel and Scharr lead to similar IQA results.

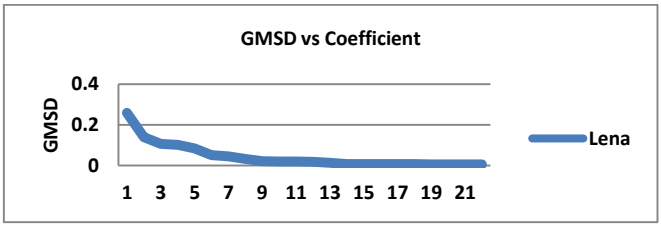

Fig 5.2.4:- figure shows the graph of GMSD vs Coefficient.

Gradient magnitude similarity deviation is low for good quality images. Graph shows the GMSD Evaluation parameter vs coefficient of images. In the coefficient between 19-21 GMSD Parameter is reached to level zero. That means only coefficient

20-23

5. PSNR (Peak signal-to-noise ratio):- PSNR, is a designing term for the proportion between the most extreme conceivable force of a sign and the force of aggravated commotion that influences the precision of its representation. Since numerous signs have a wide element range, PSNR is normally communicated regarding the logarithmic decibel scale. PSNR is most normally used to gauge the nature of remaking of lossy pressure units (e.g., for picture pressure)

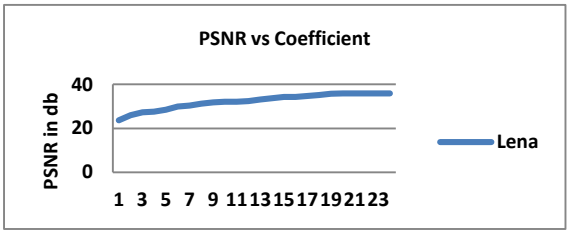

Fig 5.2.5:- figure shows graph of PSNR vs Coefficient

For Good quality images have PSNR value is high. Graph shows that the PSNR value is 35-37 in coefficient between 17-27.and its not increases rapidly for increasing the coefficient value. So for we can take only 20-25 coefficient for regeneration of compressed image.

6. RFSIM (Riesz-transform based Feature Similarity metric):- As per some analysis the human vision perceives an image mainly according to low level features. Based on this fact the RFSIM is proposed. The 1st order and 2nd order of these transform coefficients of the image taken as image features while a feature mask is defined as edge locations. The similarity index between the reference and distorted images is measured by comparing the two feature maps at key locations marked by the feature mask.

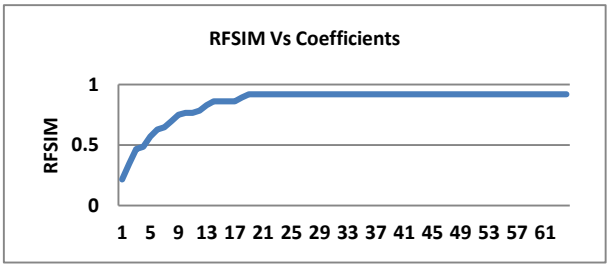

Fig 5.2.6:- figure shows graph of RFSIM vs Coefficient

In graph shows that RFSIM value is reached to the label of 0.8-0.9 in only image coefficient of between 17-29. After that coefficient, RFSIM value is constant in 0.9 for increasing the coefficient. so we can say that RFSIM value are approximately good for coefficient of 21-25.

7. SSIM (Structural-similarity-based image quality assessment):-

Regular picture signs are exceedingly organized: their pixels display solid conditions, particularly when they are spatially proximate, and these conditions convey imperative data about the structure of the items in the visual scene. The Minkowski slip metric is taking into account point shrewd sign contrasts, which are free of the basic sign structure. Albeit most quality measures in view of lapse affectability disintegrate picture signs utilizing straight changes, these don't evacuate the solid conditions, as examined in the past area. The inspiration of our new approach is to locate a more straightforward approach to look at the structures of the reference and the bended signs.

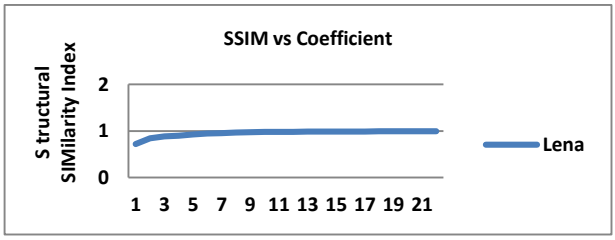

Fig 5.2.7:- figure shows graph of SSIM vs Coefficient

In this graph we shows that the feature SSIM

evaluation parameter are obtaion 1 and above in the coefficient of 11-21.then we can say that only 20-25 coefficient can provide good SSIM parameter value.

5.3 Comparative Analysis: This graph shows comparative analysis of all the evaluating parameter. So we can conclude that all the approximate value of parameter can be obtain in coefficient of 20- 25.

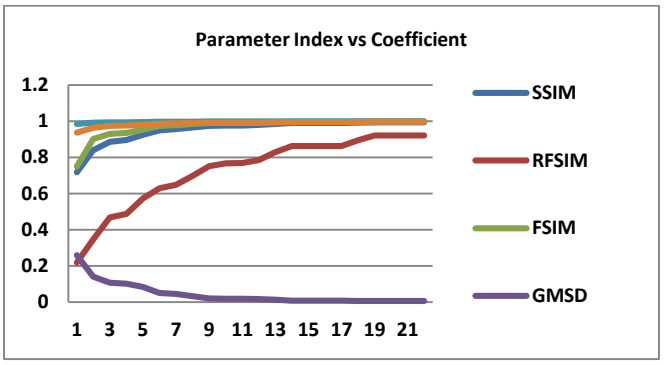

Fig 5.3.1:-comparative analysis of all parameters

5.4 Proposed Error resilient Approach Analysis at Algorithm level:

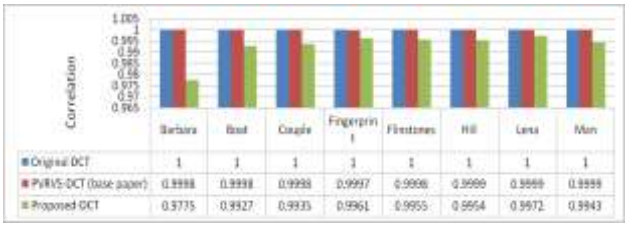

Fig 5.4.1:- Comparison of correlation between different images in different Approach.

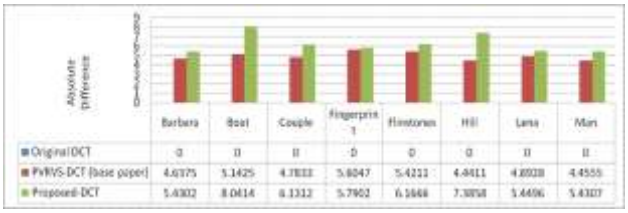

Fig 5.4.2:- Comparison of Absolute Difference for different images in different Approach.

Fig 5.4.3:- Comparison of GMSD parameter for different images in different Approach

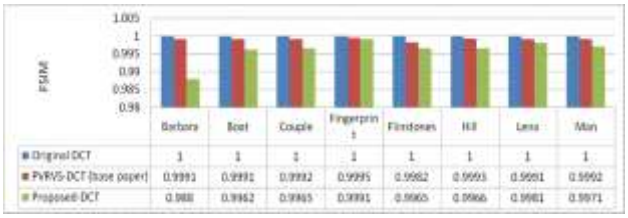

Fig 5.4.4:- Comparison of FSIM parameter between different images in different Approach

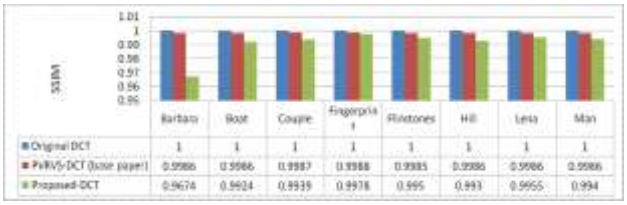

Fig 5.4.5:- Comparison of SSIM parameter for different images in different Approach

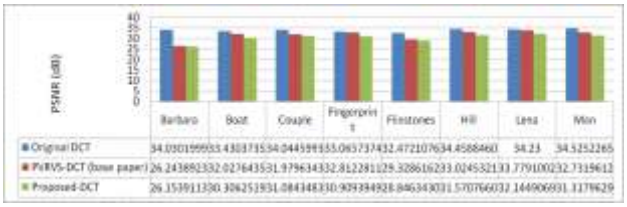

Fig 5.4.6:-Comparison of PSNR for different image in different Approach

All the graph of section 5.4 shows the comparative analysis in the hardware level for different evaluating parameter with applying different approach. Some of the parameter are greater to the previous approach & some is approximately less. We also discuss about the human eye is not sensitive to 5-10% vision, then approximation can be used where not accuracy is required. In our approach reducing the power consumption & also complexity of circuit. So the cost of this technic is less compare to other.

5.5 FPGA Analysis

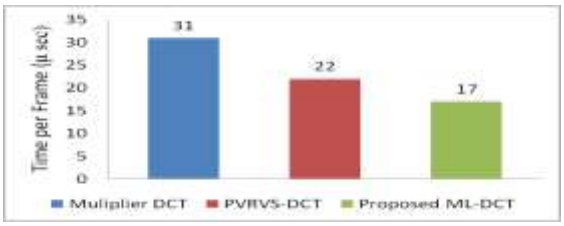

Fig 5.5.1:- figure shows the execution timing difference between multiplier DCT,PVRVS-DCT & proposed ML DCT

Now a day time is more important for all the device. If any device taking less time for the work perform than its demand is increased. Graph shows that by applying our approach then execution time per frame is less then to previous approach. Now we can say that in one frame reduced time is 31-17 = 14(us),then only one frame can reduce 45.16% time consumption . so for many frame the time consumption is also more reduced.

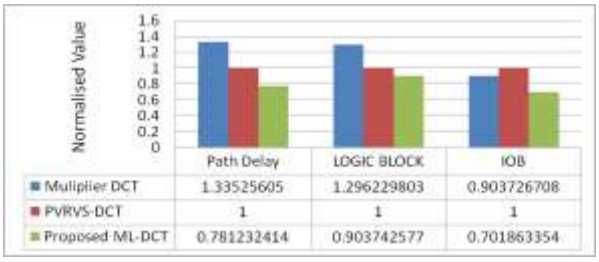

Fig 5.5.2:- figure shows the path delay, logic block & IOB different between multiplier DCT, PVRVS-DCT & proposed ML-DCT.

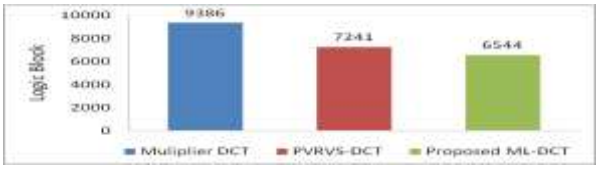

Fig 5.5.3:- figure shows the logic block is required for different approaches

Power requirement is one of the most important features for all the device.
And also more compatible device demand is more. in figure we can see that by applying our approach then requirement of logic block is less.
by mathematical analysis, previous approach (multiplier DCT) = 9386 Logic block and proposed ML-DCT = 6544 then 30.27% of logic block is reduced. If lessblock is needed then complexity can be reduced for reduction in circuit. and also power requirement is reduced. In one gate 6 transistor is needed and one block more gate are used.

Fig 5.5.4:- figure shows the input output is required for different approaches

6. CONCLUSION

The Studied DCT architecture is modified with respect to concept of error resiliency to achieve the speed, power, area & accuracy trade-off. A new design for error resiliency is proposed based on the analysis of standard image use in the digital image processing. On the basis of different quality parameter like PSNR, SSIM, etc. The architecture evolved as 20- 25 coefficient DCT architecture which is justified by implementation on algorithm in matlab and hardware level in xilinx.
The proposed architecture is implemented on Virtex-6, FPGA platform using Xilinx 14.5 and shows reduction in processing time by 20%.

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