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High Step-up Modified SEPIC Converter for Renewable Applications

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Abstract
A high step-up Dc- Dc converter based on the Modified SEPIC converter is present in this paper. This topology is the combination of a classical boost converter and a conventional SEPIC converter. The Modified SEPIC converter used for low input voltage and high output voltage applications. The theorectical analysis shows that it is suitable for the applications such as a renewable power sources with low DC output voltage The operational analysis and the design is done for the 100W power output of the modified converter. The solution is proved by MATLAB/SIMULINK.

1. Introduction

Energy shotage and environmental pollution have been the major problems for the development of human beings. The bulk use of fossil fuels, such as, oil ,gas and coal produce large environmental problems. Recently, energy generated from clean, efficient, and environmental-friendly sources have become one of the major challenges for engineers and scientists. So the renewable sources are the only solution for that. Some example of renewable energy sources are low power wind turbine, photovoltaic (PV)modules and other applications as fuel-cells, embedded systems, portable electronic equipments, uninterruptable power supply and battery powered equipment.. These applications demand high step-up static gain, high efficiency and reduced weight, volume and cost.

The use of renewable energy is increasing day by day. So many industrial applications require dc – dc converter with high boost ratios. The modified SEPIC can be used for PV energy generation in grid connected systems using AC module. In the case of residential applications energy generated by a PV module is given to the grid through the DC-DC converter[3].The main techniques used to obtain high static gain is presented in [1].Non isolated high static gain DC-DC converter are based on boost topology with coupled inductor[2],voltage multiplier cells and switch capacitor[4],switched inductor [5]and also the combinations of voltage multiplier with coupled inductor[6]-[8].A review of such non isolated high static gain DC-DC converters are present in[1]-[2].

The main topology presented in this paper is the modification of classical SEPIC converter.And operational characteristics are also presented. The theoretical and experimental analysis of the modified SEPIC DC-DC converter is developed in this paper for low DC input voltage and high output voltage applications.

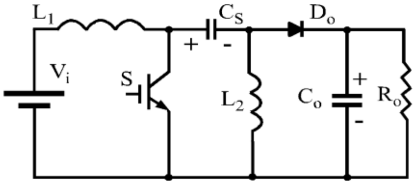


Figure. 1 Conventional SEPIC converter

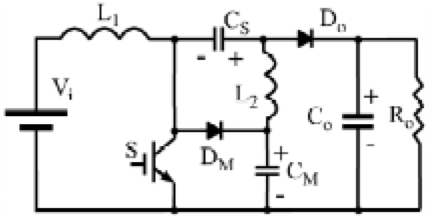


Figure. 2 Modified SEPIC converter

2. Proposed Converter

A classical SEPIC converter circuit is shown in Fig.1. Such a converter produces the step up and step down high static gain operational characteristics. In the case of SEPIC converter switch voltage is the sum of input and output voltage and static gain is lower than that obtained through conventional boost converter.The power circuit diagram of modified SEPIC converter is presented in Fig.2.In the modified SEPIC converter consist of two addional components as compared to SEPIC converter it include the diode D_M and the capacitor C_M. It consists of two inductors L_1 and L_2, two diodes D_0 and D_M.

2.1 Basic Operating Principles

Operational characteristics of modified SEPIC converter is different from classical SEPIC.The polarity of the C_S capacitor voltage is inverted and output voltage of classical SEPIC converter is used tocharge the capacitor C_M.

The continuous conduction mode (CCM) is presented in this paper.Modified SEPIC have two operational stages.

The semiconductors are consider as ideal for analysis.

1) State 1(t_0 - t_1): Fig.3 shows first operational stage.Switch S is turned–off at the instant t_1.The energy stored in the inductor L_1 is transferred to the output through the capacitor C_S and output diode D_0 .It is also transferred to the capacitor C_M and the diode D_M..Here the switch voltage is same as C_M capacitor voltage.At the same time energy stored in the inductor L_2 is transferred to the outps$_s$ut through the diode D_0 .

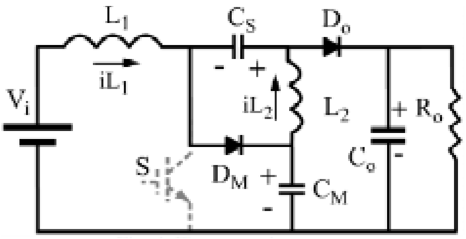


Figure 3. First state (switch off)

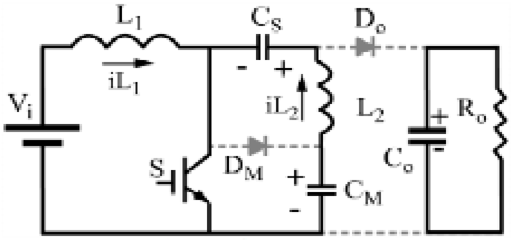


Figure 4 . second state (switch on)

2) State 2 (t_1 - t_2): Fig.4 shows second operational stage.At the instant t_1 switch S is turned on and the diodes D_0 and D_M are in reverse biased condition.The inductors L_1 and L_2 store energy.Input voltage is applied to the inputindutor L_1 and the voltage (V_{CS}-V_{CM}) is applied to the inductor L_2.The voltage V_{CM} is greater than voltage V_{CS}.

The main theoretical waveforms are presented in Fig. 5.

The maximumvoltage in all diodes and in the power switch is equal to the C_M capacitor voltage the output voltage is equal to the voltage across the capacitors C_S and C_M.Input current equal to the average current in inductor L_1 and output current equal to the average current in inductor L_2.In the CCM mode, static gain of modified SEPIC converter is presented in (1) and it is higher than that obtained from classical boost converter.

$$\frac{V_O}{V_i} = \frac{1+D}{1-D} \qquad (1)$$

The voltage across the capacitor C_M is given by the equation (2) and is same as the output voltage of the the boost converter.The maximum switch voltage is equal to the voltage V_{CM} and is lower than converter output voltage.

$$\frac{V_{CM}}{V_i} = \frac{1}{1-D} \qquad (2)$$

The voltage across the capacitor C_S is given by (3)

$$\frac{V_{CS}}{V_i} = \frac{D}{1-D} \qquad (3)$$

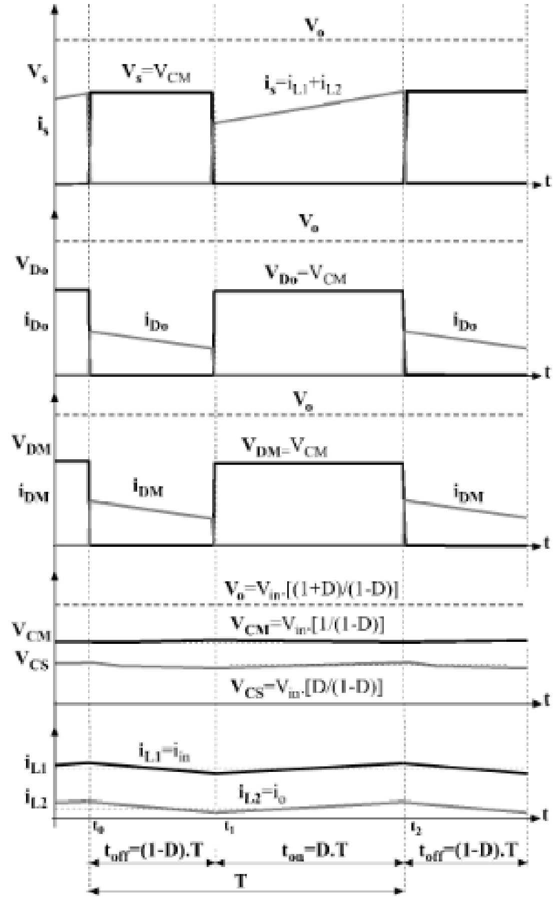


Figure 5. Main theoretical waveforms

3. Design Considerations of the Proposed Converter

Considering the following specifications:

Output power ,P_O =100 W
Input voltage,V_i =12V
Output voltage,V_O =150V
Switching Frequency ,fs =24kHz

1) *Switch duty-cycle*

Form the static gain duty cycle can be calculated by (4)

$$D=\frac{Vo-Vi}{Vo-Vi}=\frac{150-12}{150+12}=.85185 \qquad (4)$$

2) *Switch and diodes voltages*

Switch and the diode voltages are the same and is given by (5)

$$Vs=V_{Do}=V_{DM}=\frac{V_i}{1-D}=\frac{12}{1-.85185}=80.99 \qquad (5)$$

3) *L_1 and L_2 inductance*

As the basic sepic, boost, and the modified sepic converters present the same input stage, the equation for the determination of the input current ripple is the same for all converters. The input current ripple (Δi_{L1}) during theconduction of the power switch is defined by the following equation.

$$\square i_{L1}=\frac{V_i D}{L_1 f_S} \qquad (6)$$

Where, f is the switching frequency.The input current ripple Δi_{L1} considered is 18% of the peak input current (i_{inpk}). Therefore, the input current ripple is calculated as follows:

$$\Delta i_{L1}=i_{inpk}\times .18=2.121A \qquad (7)$$

Input inductance can be calculated by the following equation

$$L_1=\frac{D\times V_i}{f_s\times \Delta i_L}=\frac{.85185\times 12}{24000\times 2.121}=.020mH \qquad (8)$$

For the simulation L_2 taken as the half of input inductor.

$$L_2=.0104 \qquad (9)$$

4) *Capacitors C_S and C_M*

The capacitors C_S and C_M have the same voltage ripple.□□□The capacitance can be calculated by the capacitor charge variation, considering null the capacitor series equivalent resistance. Normally, a small capacitance value is obtained and a capacitor with low series equivalent resistance can be used. Considering a capacitor voltage ripple ΔV_C equal to 10% of the nominal voltage of theC_M capacitor, the capacitance can be calculated by the following equation

$$C_S=C_M=\frac{I_O}{\Delta V_C\times f_S}=\frac{.667}{24000\times 8.099}=3.43\mu F \qquad (10)$$

Where

$$\Delta V_C=\frac{V_i}{1-D}\times\frac{10}{100}=\frac{12}{1-.85185}\times .1=8.099V \qquad (11)$$

1) *Output capacitor Co*

The output filter capacitance is defined by a function of the output power P_o, the supply i.e. grid frequency f, and the low frequency output voltage ripple ΔV_o. The output voltage ripple is considered equal to 1% of the output voltage in calculation. The output capacitance is calculated as given below:

$$C_O=\frac{P_O}{2\times\Pi\times f_G\times 2\times V_O\times\Delta V_O}$$

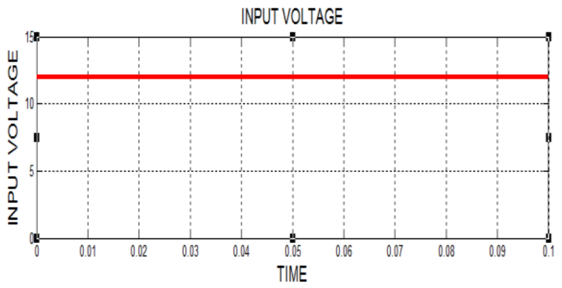
$$=\frac{100}{2\times\Pi\times 50\times 2\times 150\times 150\times .01}=.070735mF$$

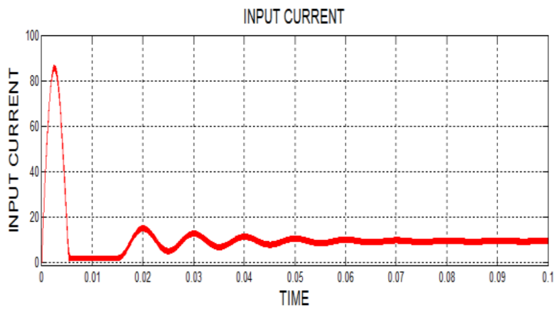
3.1 Simulation Results

Before this section is discussed, specifications of the converter given as, (1) the rated DC input voltage is 12V; (2) the rated DC output voltage is 150V; (iii) the rated DC output power is 100W; (iv) the switching frequency is 24kHz; (v) Inductor values taken as .02mH and .0104mH; (vi).07073mF capacitor is chosen for C_0.

The closed loop Simulink model for the modified SEPIC converter was used. A 12V DC voltage is the input of the modified SEPIC.

Fig.6. shows the simulation results of modified SEPIC converter. The operation of this converter is verified here. At 85.18% duty cycle, input of 12V produces an output of 150V . Both the inductor currents are obtained with ripples .





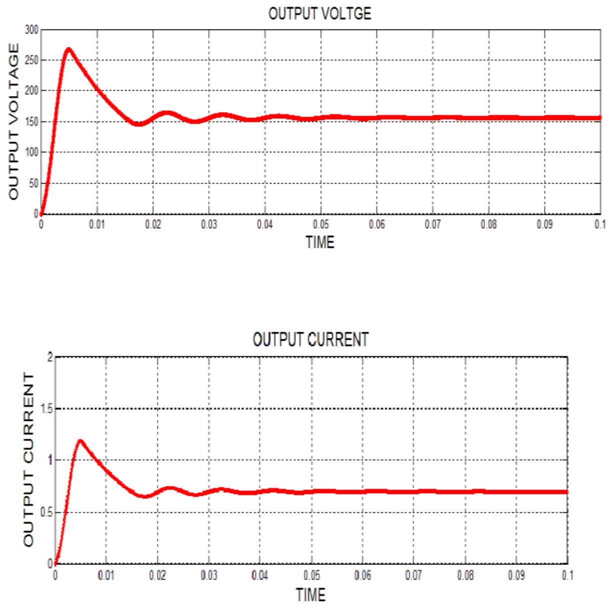


Figure 6. Simulation Results of modified SEPIC converter

4. Conclusion

A high efficiency dc-dc converter with a combination of conventional boost converter and a SEPIC converter is proposed in this paper. This converter can achieve high voltage gain. A modified SEPIC converter is analyzed and designed. The converter model is simulated on Simulink for closed loop

5. Future work

As future work, hardware for the proposed converter can be developed. Furthermore this converter can be designed for various voltage levels.

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