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Design and Implementation of High-Speed Low Power Multipliers Using Reversible Logic

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ABSTRACT
Reversible logic is one of the promising research areas in low power applications such as quantum computing, optical information processing, DNA computing and also thermodynamic technology, Nanotechnology and low power CMOS design. In this paper, a novel Reversible logic gate has been proposed and novel architecture for multiplier is constructed by using ANU gate and PERES gate. A Multiplier is one of the key hardware blocks in most fast processing system which is not only a high delay block but also a major source of power dissipation. Power dissipation for Reversible logic gates is very less because of its reversibility property. The main purposes of designing reversible logic are to decrease quantum cost, depth of the circuits and the number of garbage outputs. The primary characteristics like garbage outputs, Constant inputs and number of gates got decreased. The logical calculations also got decreased.
Keywords: *Reversible logic, Reversible gate, Power dissipation, Garbage, Quantum cost, T-Spice v13.0 (Tanner Tools)*

INTRODUCTION

In modern era decreasing power and increasing speed are two major concerns for any VLSI design. Usually in Irreversible gates there is no one to one mapping between the outputs and inputs and power dissipation is high and also leakage of power is high. So we are going towards the new logic called the Reversible logic. Power dissipation is one of the important problems faced now a day in VLSI design [1]. According to Landauer's principle, The combinational circuit dissipates KTlog2 [1] Joules of heat for every bit information to be lasted, irrespective of the technology used where K is Boltzmann constant and T is temperature. Heat dissipation reduces the life span of the circuits. The information gets lost when input bits are not able to recover from the output vectors. Reversible gates unsurprisingly take care of heat, since input vectors are uniquely recovered from the output vectors. Each output of the Reversible gates is used once, thus Reversible circuit is feedback free. All computations which are considered to be quantum are necessarily to be Reversible. All logic gates like AND, NOR, NAND, OR, EXOR etc are not Reversible except NOT gate. This paper describes the design and implementation of 4x4 bit Reversible multiplier based on CMOS technology using EDA (Electronic Design Automation) tool.

THE CONCEPT

Reversibility in computing means that no information about the computational states can ever be lost, so we can recover any earlier state by computing backwards or un-computing the results.

This is logical reversibility. The advantages of logical reversibility can be achieved only after employing physical reversibility. Physical reversibility is a process that dissipates zero energy to heat. Absolutely perfect physical reversibility is practically Unachievable. A comprehensive review of the existing CMOS circuit design style and Reversible logic style is given, describing their advantages and limitation. Also, implementation of various 4 bit multipliers were analyzed in the terms of delay and power consumption using T-Spice.

1.2 BASICS OF REVERSIBLE LOGIC GATES

- **The number of Reversible gates (N):** The number of reversible gates used in circuit.
- **The number of constant inputs (CI):** This refers to the number of inputs that are to be maintained constant at either 0 or 1 in order to synthesize the given logical function.
- **The number of garbage outputs (GO):** This refers to the number of unused outputs present in a reversible logic circuit. One cannot avoid the garbage outputs as these are very essential to achieve reversibility.
- **Quantum cost (QC):** This refers to the cost of the circuit in terms of the cost of a primitive gate.[2]
- **Reversible logic gate:** A logic gate is said to be reversible if and only if

a. The number of inputs and number of outputs are equal to each other.
b. A one to one correspondence should present between inputs and outputs.

1.3.1 Array Multiplier

The array multiplier [2] is carried out by simple shifting and accumulation of partial products. Fig 1.Shows the 4-bit conventional array multiplier. The partial products are added by simple adder. It uses short wires that go from one full adder to adjacent full adders horizontally, vertically or diagonally [3]. An n × n array of AND gates can compute all the *i i a b* terms simultaneously. The terms are summed by an array of "n [n - 2]"full adders and „n" half adders. The shifting of partial products for their proper alignment is performed by simple routing and does not require any logic. The number of rows in array multiplier denotes length of the multiplier and width of each row denotes width of multiplicand. The output of each row of adders acts as input to the next row of adders. Each row of full adders or 3:2 compressors adds a partial product to the partial sum, generating a new partial sum and a sequence of carries.

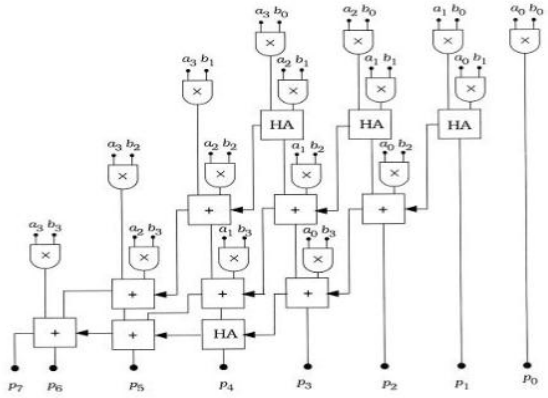


Fig .1 Block diagram of 4-bit Array Multiplier

The delay associated with the array multiplier is the time taken by the signals to propagate through the AND gates and adders that form the multiplication array. The delay of the array multiplier is given by [4].

$$(T\ critical) = [(N-1) + (N-2)]*T(Carry) + (N-1)*T(Sum) + T(AND)$$

ere T (*Carry*) is the propagation delay between input and output carry, T (*Sum*) is the delay between the input carry and sum bit of the full adder, T (*AND*) is the delay of AND gate, N is the length of multiplier operand. Fig.2 shows the CMOS logic implementation of Array multiplier.

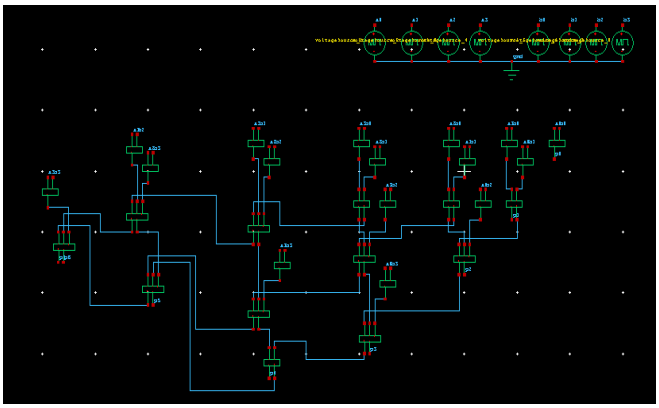


Fig. 2 Implementation of 4*4 Array multiplier using CMOS logic

Tree Multiplier

C. S. Wallace suggested a fast technique to perform multiplication in 1964 [5]. The amount of hardware required to perform this style of multiplication is large but the delay is near optimal. The delay is proportional to log (N) for column compression multipliers where N is the word length. This class of multipliers is based on reduction tree in which different schemes of compression of partial product bits can be implemented. In tree multiplier partial-sum adders are arranged in a treelike fashion, reducing both the critical path and the number of adders needed [6] as shown in the figure 3, shown below:

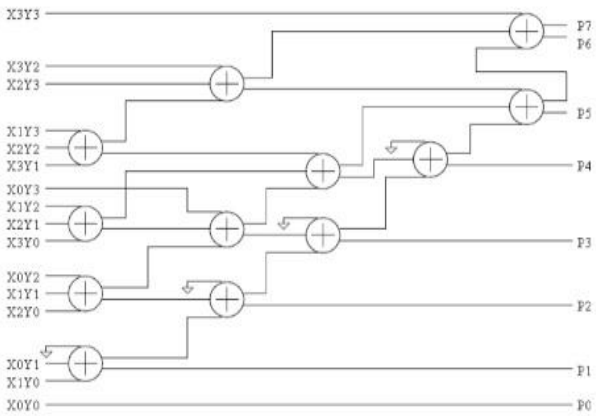


Fig .3 Block diagram of 4-bit Tree Multiplier

The partial products or multiples are generated simultaneously by using a collection of AND Gates. The multiples are added in combinational partial products reduction tree using carry save adders, which reduces them to two operands for the final addition. The results from CSA are in redundant form. Finally, the redundant result is converted into standard binary output at the bottom by the use of CPA[7]. Fig.4 shows the CMOS logic implementation of Tree multiplier.

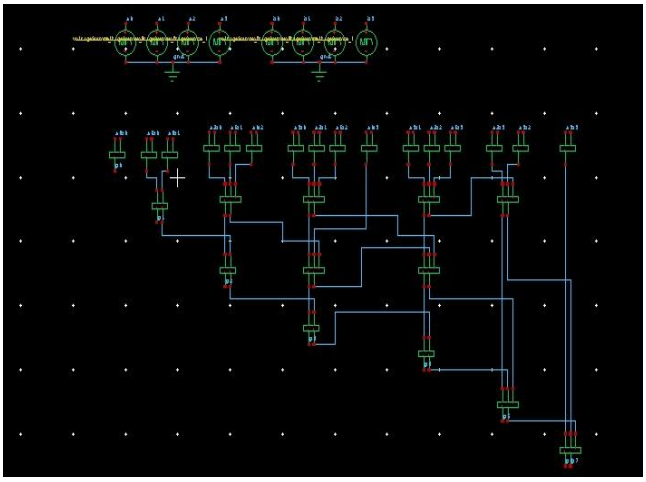


Fig. 4 Implementation of 4*4 Tree multiplier using CMOS logic

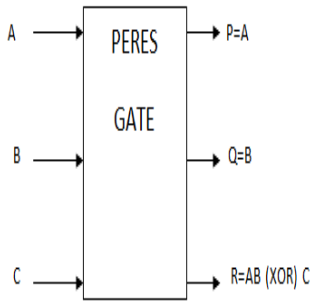
a. Reversible Multiplier

Proposed Reversible Gates

- **PERES Gate:(PG)**[8] : It is a 3x3Reversible logic gate and the Quantum cost is four. This gate can be used as a half adder circuit. The input vector and output vector are given as

I= (A,B,C) and O = (X=A,Y=A^B, Z=A.B^C)

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0



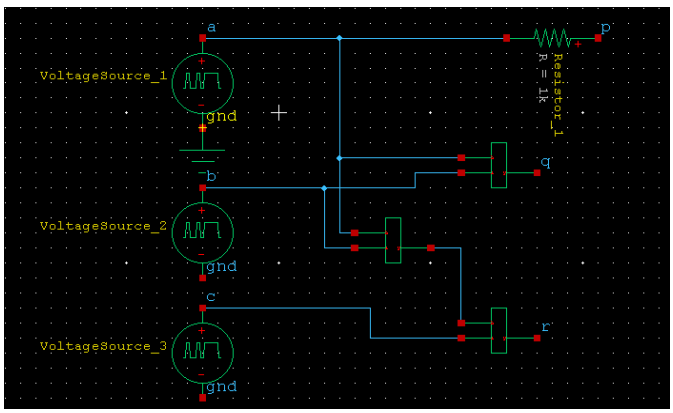
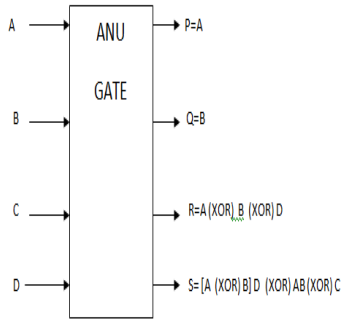


Fig .5 Block diagram, Truth table and CMOS implementation of PERES gate

- **ANU Gate:**[9] : This is our new proposed 4x4 Reversible logic gate which can mainly function as a full adder circuit. The inputs and outputs to this gate are given below

I =(A,B,C,D) and O=(P=A),(Q=B),(R=(A^B^D)), S=((A^B)&C^(A&B)^D)

A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0
0	0	1	0	0	0	0	1
0	0	1	1	0	0	1	1
0	1	0	0	0	1	1	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	1
0	1	1	1	0	1	0	0
1	0	0	0	1	0	1	0
1	0	0	1	1	0	0	1
1	0	1	0	1	0	1	1
1	0	1	1	1	0	0	0
1	1	0	0	1	1	0	1
1	1	0	1	1	1	1	1
1	1	1	0	1	1	0	0
1	1	1	1	1	1	1	0



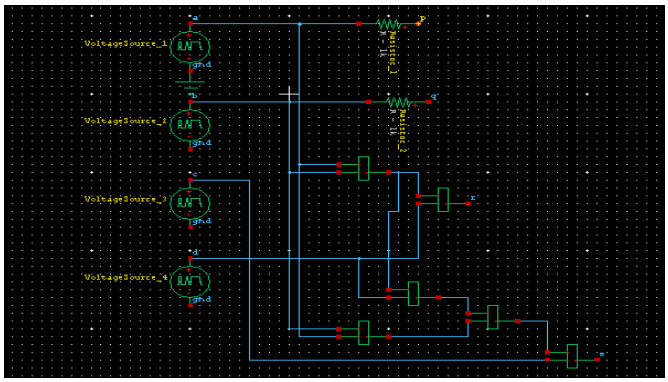


Fig .6 Block diagram, Truth table and CMOS implementation of ANU gate

b. Proposed Multiplier

In this section, a proposed architecture for 4x4 multiplier was shown in figure 7. To implement any multiplier we need adders and the adders for that multiplication has been produced by using ANU gate as mentioned above. Here for implementing a multiplier we have 2 steps are

1) Partial Product generation
2) Addition of Partial products

The steps are as follows

Step1: S0 = X0*Y0
Step2: S1 = X1*Y0+X0*Y1
Step3:S3 = X2*Y0+X0*Y2+X1*Y1
Step4:S4 = X3*Y0+X0*Y3+X2*Y1+X1*Y2
Step5:S5 = X3*Y1+X1*Y3+X2*Y2
Step6:S6 = X3*Y2+X2*Y3
Step7:S7 = X3*Y3
Finally the output is : P0P1P2P3P4P5P6P7

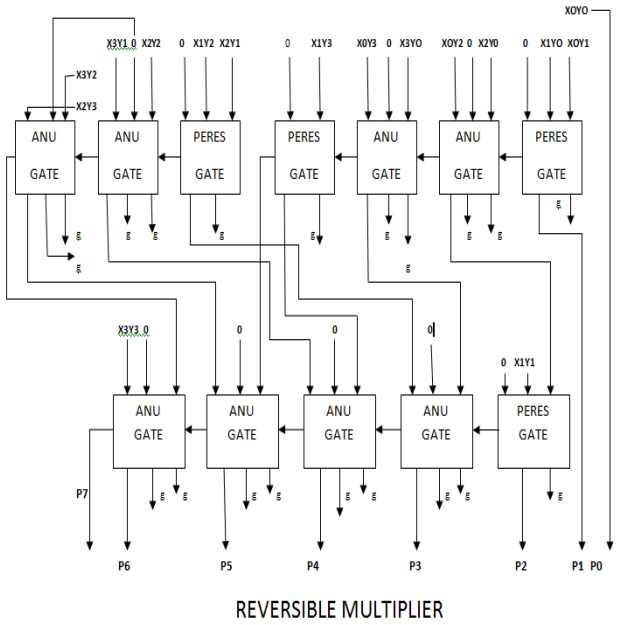


Fig .7 Block diagram of proposed 4-bit Reversible Multiplier

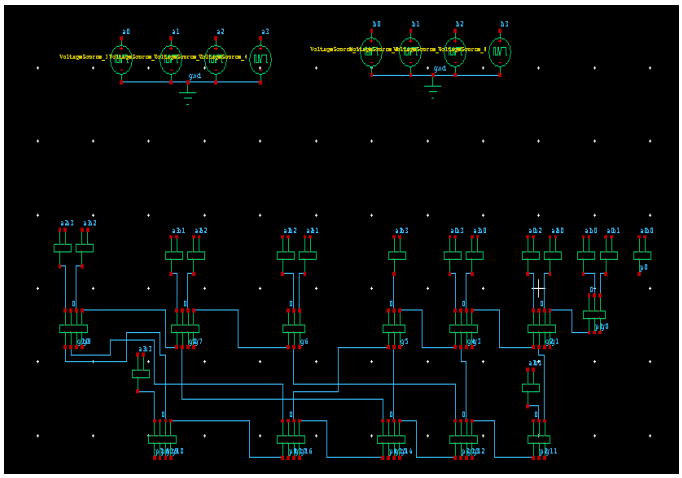


Fig. 8 Implementation of 4*4 Reversible multiplier using CMOS logic

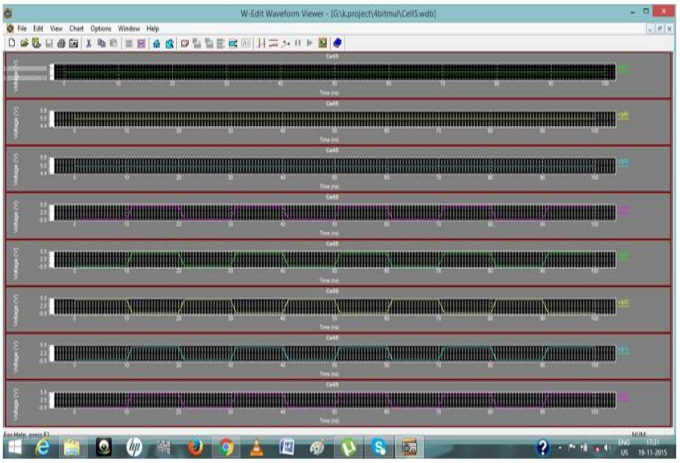


Fig. 9 Wave form of 4*4 Reversible multiplier using CMOS logic

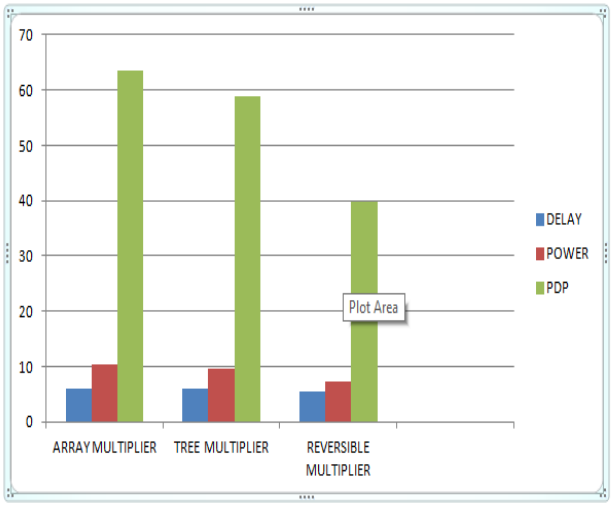
PERFORMANCE PARAMETERS AND SIMULATION SET-UP

The 4*4 bit Reversible multiplier is compared based on the performance parameters like propagation delay, average power consumed, and number of transistor. To achieve better performance, the circuits were designed using CMOS logic process compare 4*4 Reversible multiplier with Array multiplier and Tree multiplier in term of propagation delay, average power consumed ana power delay product. All the circuits have been designed using TANNER EDA with Model file as **dual.md** [10]. The power estimation is a difficult task because of its dependency on various parameters and has received a lot of attention. Direct Simulation method is used in order to analyse the results. Table 1 Shows Comparative Experimental results of 4*4 Reversible multiplier using CMOS logic styles and also compared with conventional method multiplier in terms of power and delay and power delay product.

Table 1

LOGIC STYLE	DELAY(ns)	AVERAGE POWER CONSUMED(mwatts)	POWER DELAY PRODUCT(pJ)	AREA / NO OF TRANSISTORS
Array Multiplier(CMOS)	6.1159	10.38	63.48	400
Tree Multiplier(CMOS)	6.1014	9.63	58.75	400
Reversible Multiplier(CMOS)	5.39	7.39	39.83	776

Fig. 10 Comparsion of 4*4 Reversible Multipler using CMOS with Array multiplier and tree multiplier using CMOS in terms of delay, averged power consumed and power delay product are shown.



RESULT ANALYSIS

It has been observed that 4*4 Reversible multiplier is better than 4*4 Conventional Multiplier and Tree Multiplier. It helps a person to solve problems faster. It provides one line answer. Time saved can be used to answer more questions. It better in terms of Propagation Delay, Average Power Consumed and Power Delay Product (PDP). In terms of propagation delay in Reversible Multiplier in CMOS logic style is 5.39 ns and In Array multiplier Propagation Delay id 6.1159ns.As a conclusion 4*4 Reversible Multiplier is better than Array multiplier in terms of Propagation Delay.

CONCLUSIONS

This paper presents multiplication based on Reversible Logic. The design of the 4x4 bit Reversible multiplier is Implemented on T-Spice v13.0. It is a method for hierarchical multiplier design which clearly indicates the computational advantages offered by Reversible methods. Using CMOS logic computational path delay is found to be 5.39ns but for multiplier using conventional method(Array) computational path delay is found to be 6.1159ns. Hence it can be concluded that the performance of the 4x4 bit Reversible multiplier seems to be highly efficient in terms of speed when compared to Conventional multipliers. Reducing the time delay is very essential requirement for many applications and Reversible Multiplication technique is very much suitable for this purpose.

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